MSU FREND Hardware Interface

This is a collection of documents describing the Michigan State University's hardware interface between our Control Data 6000 mainframe and the attached Interdata 7/32 front-end minicomputer. The 7/32 ran a proprietary MSU-written operating system called FREND.

The hardware interface was designed in 1974 - 1976 by Dr. Lewis Greenberg, who retired as Director of the MSU Computer Laboratory in 2002. The interface was constructed and debugged by MSU engineer Peter Chen, who still works for the Computer Lab as of this writing.

These documents were lent to me by Tim Childs, a colleague of Peter Chen. They came in several folders, most notably two folders named "7/32 Front-End (A)" and "7/32 Front-End (B)". I don't know what the difference is between (A) and (B).

Contents

- Schematic: Full Front-End System
- Cyber 750 Front-End Block Diagram
- 7/32 Front End Interface - 10 pages describing the interface, focusing on flag bits. This was in the Front-End (A) document
- FEI - 5 pages describing the function codes. This was in the (B) folder.
- 750 Front-End Devices - 7-page 1986 listing
- 23 pages of flow charts and boolean equations describing status bits. From Front-End (A).
- 15 pages of detailed, gate-by-gate diagrams with IC part numbers. Photoreduced and difficult to read. From (A).
- 16 pages of flow charts, possibly from (B).
- DAA Board Layout (For Vadic Coupler).
- 6 pages of handwritten tables on lined paper describing chassis layout, connectors, and "PALS", including phone number assignments.
- Phone Line[s] for VADIC Coupler

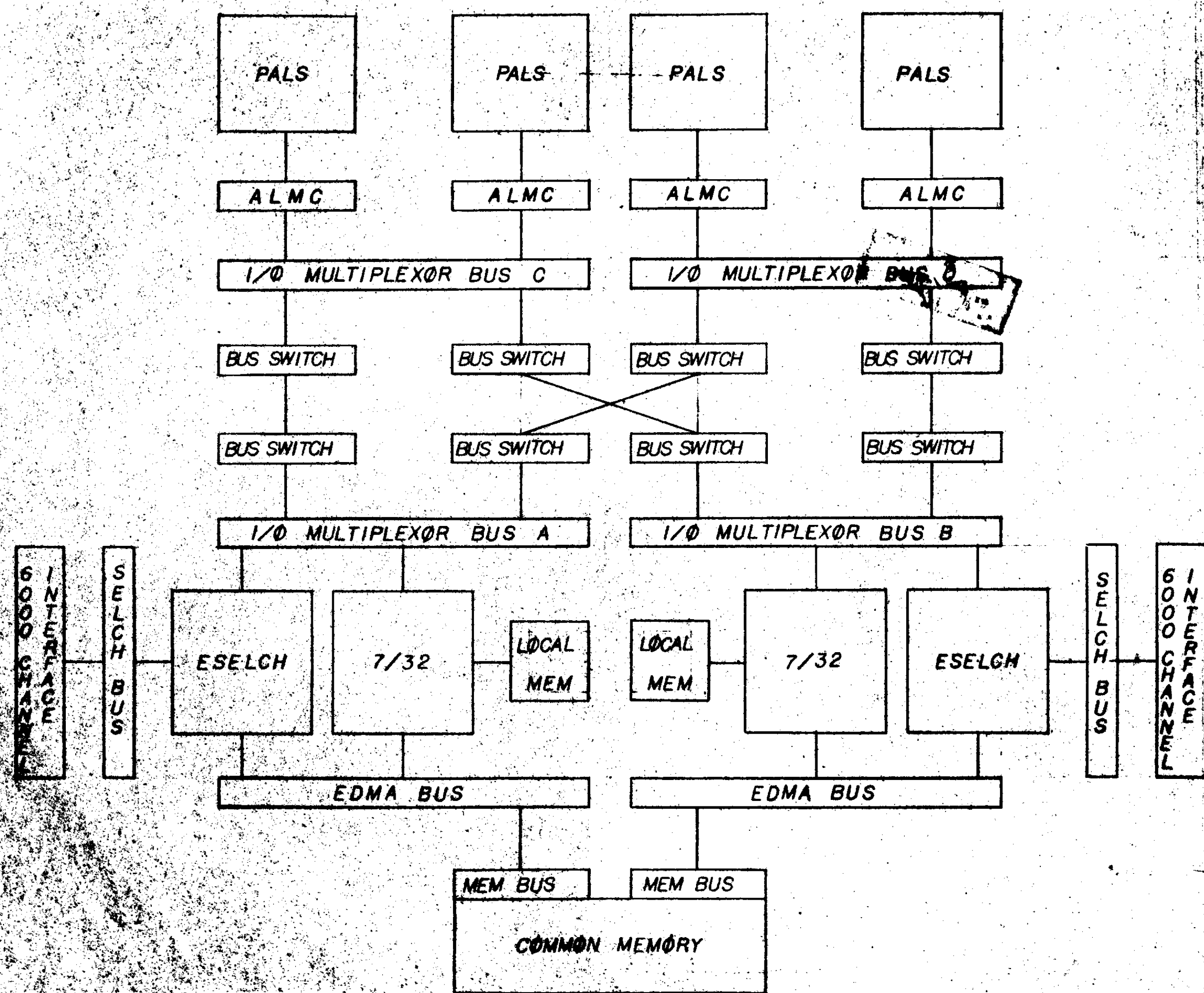
Although this documentation is so detailed that it would seem to leave little to the imagination, in fact I have omitted most of the extremely detailed documentation. The omitted material includes:

- A lengthy computer printout that seems to include IC part numbers and their relationships to each other.
- A great deal of other material which did not seem interesting to me.

(This list is not complete, because I did not bring these omitted items home with me from MSU.)

Also see the "6SM" software documentation, to be made available separately.

Mark Riordan   mrr *at* msu.edu   December 2003



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

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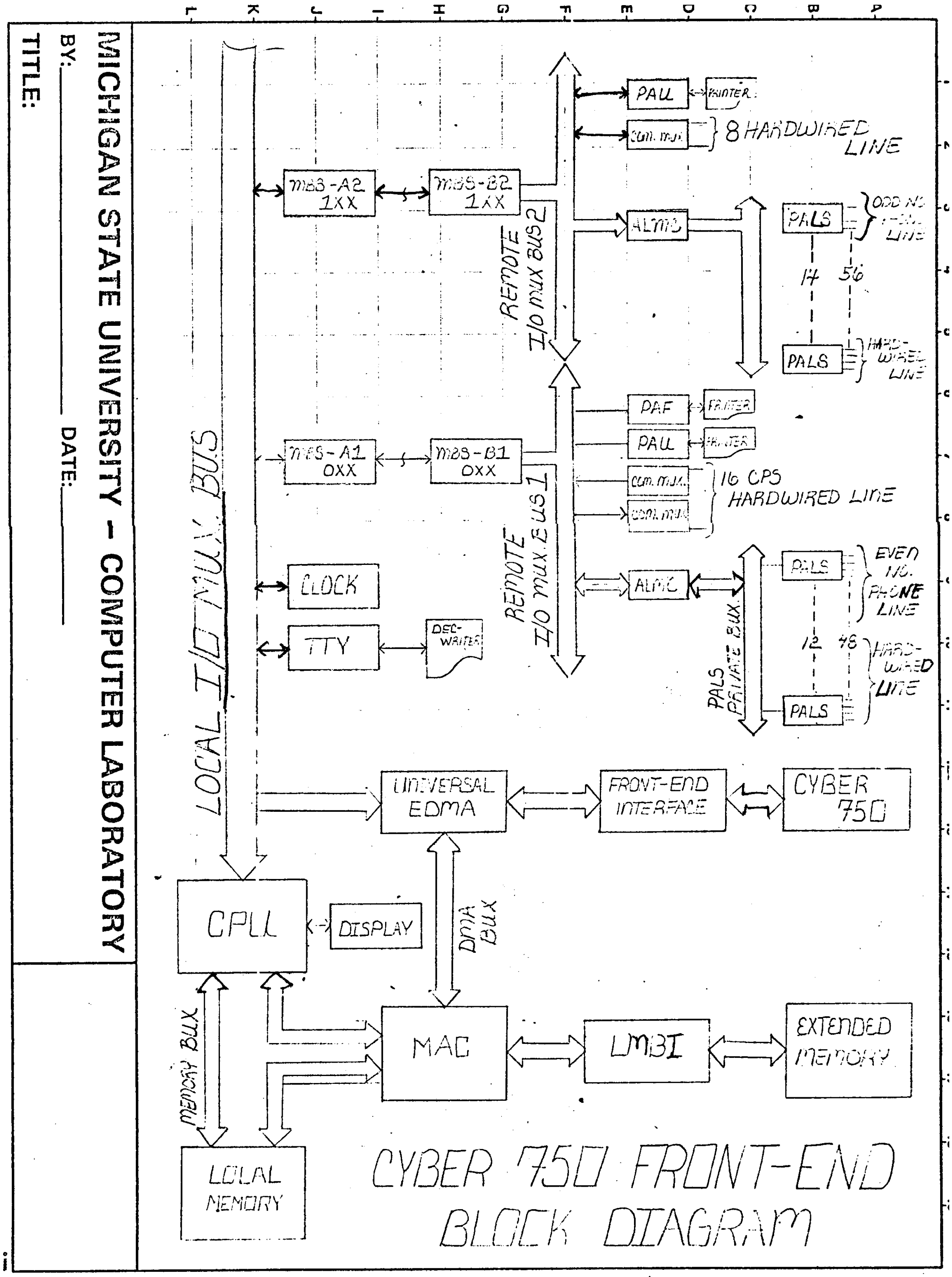
TITLE— FULL FRONT-END SYSTEM



MICHIGAN STATE UNIVERSITY – COMPUTER LABORATORY
BY:
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TITLE:
LOCAL I/O MUX BUS
MBS-A2 1XX
MBS-B2 1XX
REMOTE I/O MUX BUS 2
PAU
PRINTER
COM. MUX
8 HARDWIRED LINE
ALMC
PALS
14
56
PALS
MBS-A1 0XX
MBS-B1 0XX
REMOTE I/O MUX BUS 1
PAF
PRINTER
PAU
PRINTER
COM. MUX
COM. MUX
16 CPS HARDWIRED LINE
CLOCK
TTY
DEC-WRITER
ALMC
PALS
EVEN NO. PHONE LINE
12
48
HARD-WIRED LINE
PALS PRIVATE BUX
PALS
UNIVERSAL EDMA
FRONT-END INTERFACE
CYBER 750
DMA BUX
CPU
DISPLAY
MEMORY BUX
MAC
LMBI
EXTENDED MEMORY
LOCAL MEMORY
CYBER 750 FRONT-END BLOCK DIAGRAM

7/32 Front End Interface

INTRODUCTION

The front end interface between the CDC 6000 peripheral processor (PP) and the Interdata 7/32 has been designed to allow maximum flexibility in communication and data transfer between the two computers.

The interface allows the 6000 PP to effectively deadstart the 7/32, to issue interrupts to the 7/32, and to read status information from the 7/32. It provides for data transfer using either (1) the high speed direct memory access (DMA) capabilities of the 7/32 selector channel (SELCH) or (2) normal, lower speed I/O operations of the 7/32 I/O multiplexor bus.

Information is sent and received by the 6000 PP via the 6000 channel. The interface appears as a single piece of equipment on the 6000 channel and all communications information (interrupts, status, etc.) and data is transferred through the one port.

The 7/32 communicates with the 6000 PP by setting and reading status bits, receiving and acknowledging interrupts, and by setting bits in the SP-BITS (system program bits) register (which can be read by the PP). The normal read and write data instructions (RD, WD, etc.) are used for transferring data to or from the interface. High speed (DMA) access is available since the 7/32 interface is connected to the selector channel (SELCH).

The interface appears as two separate devices on the 7/32 I/O bus. Both devices are connected to the 7/32 via the selector channel (SELCH). By using the SELCH connection data can be transferred using one of two methods; the 7/32 may use the high speed direct memory access (DMA) feature by sending start, stop, and address commands to the SELCH, or the 7/32 can use the SELCH as a simple extension of the I/O multiplexor bus. The two device connections from the interface have device numbers nnnnnnn0 and nnnnnnn1. The seven most significant bits of the device numbers are the same and are set upon installation of the interface. Device nnnnnnn0 is responsible for data transfer between the 7/32 and the PP and for interrupts caused by data transfer (described later). Device nnnnnnn1 handles interrupts originated by the PP and their associated communication. Fiqure 1 shows a block diagram of the basic connections.

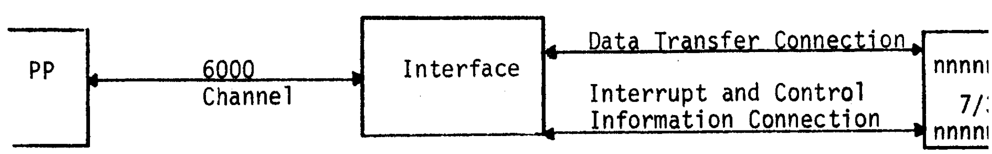


Figure 1

DATA TRANSFER

There are six "mode" flags (flip-flops) associated with data transfer. Each of these can be set or reset only by using the 7/32 output command instruction. The state of each of the "mode" flags can be determined by the PP through a status request. A description of these flags follows:

MODE - MODE2 Flags

These flags signal the format to be used when transferring data between the PP and 7/32. The "MODE" flag signals how many PP bits are to be used.

MODE = 0 => use whole PP word

MODE = 1 => use PP word as 2 six bit bytes.

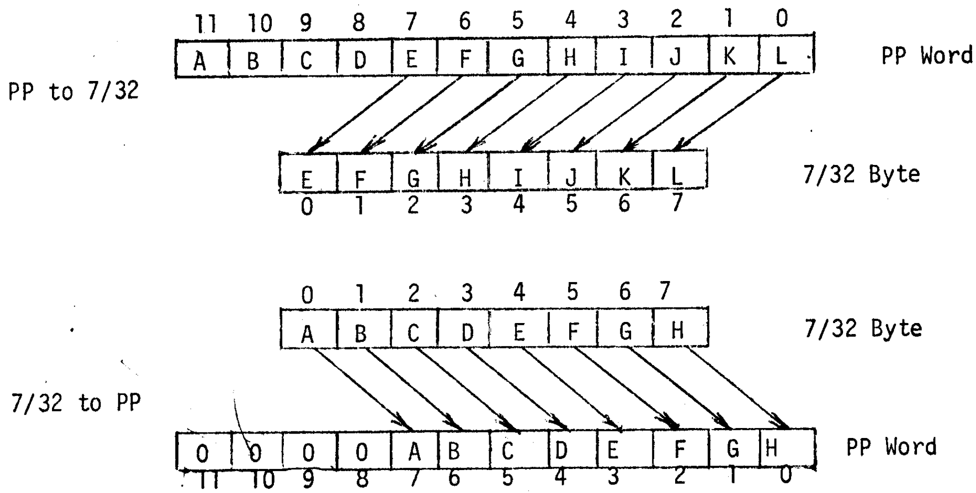
The "MODE2" flag signals whether byte or halfword mode is to be used by the 7/32.

MODE2 = 0 => use 7/32 byte mode

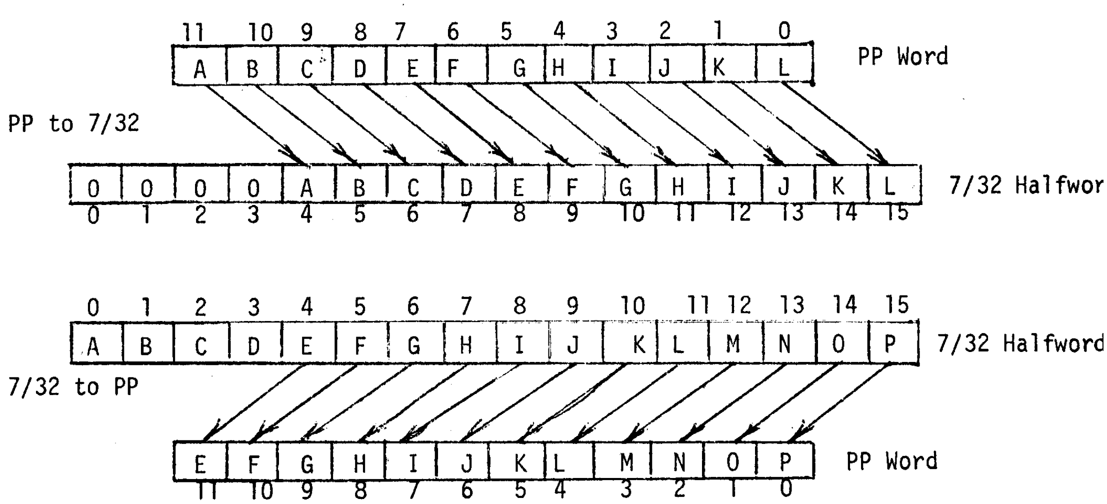
MODE2 = 1 => use 7/32 halfword mode.

Thus there are four possible data formats as follows:

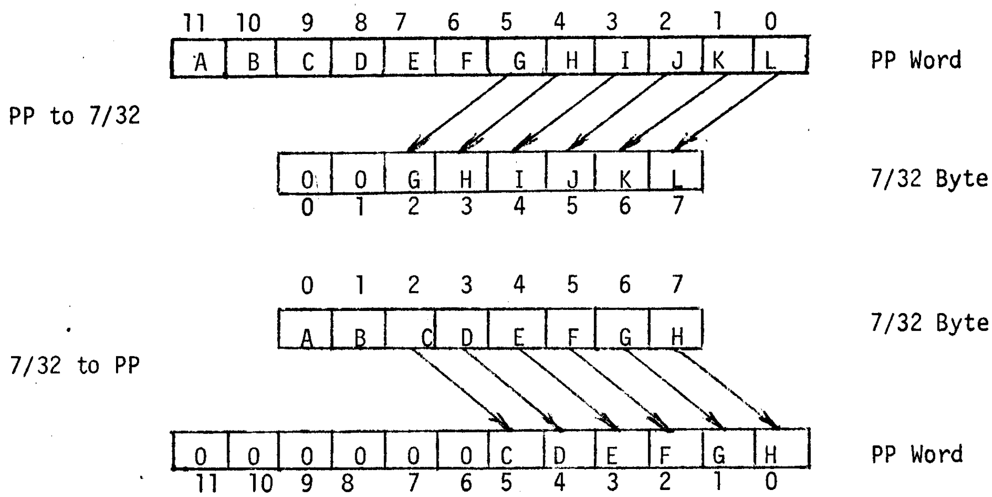
MODE = 0, MODE2 = 0



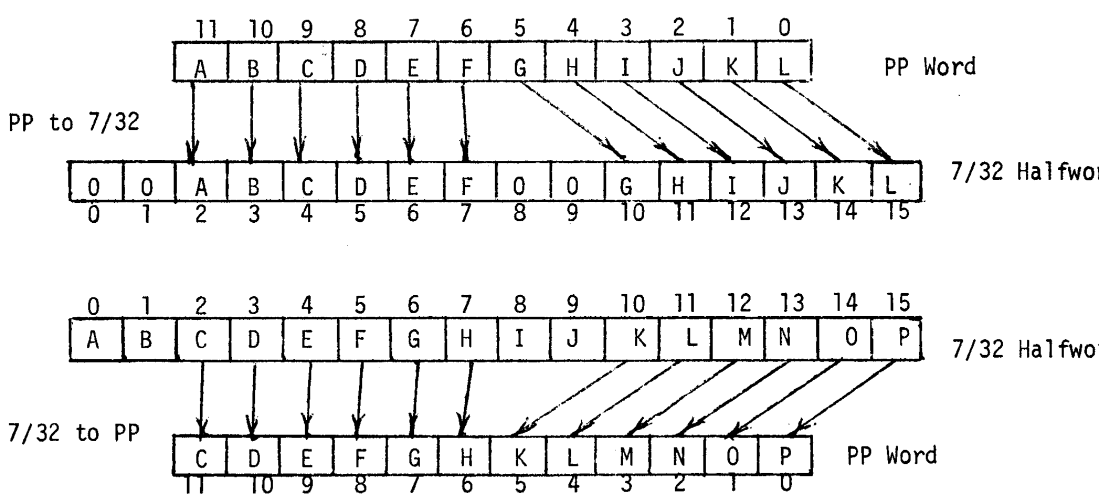
MODE = 0, MODE2 = 1



MODE = 1, MODE2 = 0



MODE = 1, MODE2 = 1



IN-MODE - OUT-MODE Flags

These flags signal the current direction of data flow through the interface as shown in the table below.

	OUT-MODE=0	OUT-MODE=1
IN-MODE=0	No Data Transmission expected	Data is expected from 7/32 to PP
IN-MODE=1	Data is expected from PP to 7/32	Illegal Cannot be Set

When the IN-MODE flag is set the interface expects to receive data from the PP. Associated with the input circuitry is a 12 bit holding register INPUT-65 and its corresponding full flag IN-65. When a full is received from the PP channel (data is on the channel) and the holding register INPUT-65 is free (IN-65 is reset) the data is transferred to INPUT-65 and IN-65 is set. An empty signal is then returned to the PP channel. If IN-65 is already set when the full is received from the channel the channel will hang until IN-65 is cleared. IN-65 is cleared by a 7/32 read request (or a DMA read request) to device nnnnnnn0. The form of the data received by the 7/32 depends on the setting of the MODE and MODE2 flags.

When the OUT-MODE flag is set the interface expects to send data to the PP channel. Associated with the output circuitry is a 16 bit holding register OUTPUT-32 and its corresponding full flag OUT-32. When the channel is active and OUT-32 is set data is sent to the PP from OUTPUT-32. The format of the data sent is dependent upon the setting of the MODE and MODE2 flags. When a empty is received from the PP, OUT-32 is cleared. OUT-32 is set by a 7/32 write request to device nnnnnnn0. If a 7/32 write request is issued when OUT-32 is set (data is already in OUT-32) the 7/32 will hang until OUT-32 is cleared. If the PP tries to input data from the interface and OUT-32 is not set the PP channel will hang until data becomes available (OUT-32 becomes set).

RT Flag

When the RT flag is set an interrupt is sent to the 7/32 by device nnnnnnn0 whenever one of the following conditions occurs.

1) IN-MODE=1, IN-65=1
   That is, there is data available for the 7/32.

2) OUT-MODE=1, OUT-32=0
   That is, data from the 7/32 is needed by the interface.

When the RT flag is reset no interrupts will occur on device nnnnnnn0.

ST-32 Flag

When the ST-32 flag is set the IN-MODE and OUT-MODE flags are ignored. Instead of providing I/O operations the interface provides 16 bits of general status on device nnnnnnn0 whenever a halfword is read by the 7/32. Resétting the ST-32 flag returns the interface to normal operation. The bits returned by the read in status mode are as follows.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			ST-65	IN MODE	OUT MODE	MODE	MODE2	$\overline{\text{ACT-65}}$	$\overline{\text{IN-65}}$	$\overline{\text{OUT-32}}$	IP	BUSY	RT		DACT

WHERE:	BIT
undefined	0
undefined	1
undefined	2
5T-65=1 if PP is in status mode	3
IN-MODE=1 if IN-MODE is set	4
OUT-MODE=1 if OUT-MODE is set	5
MODE=1 if MODE flag is set	6
MODE2=1 if MODE 2 flag is set	7
$\overline{\text{ACT-65}}$ = 1 if 6000 channel not acitve	8
$\overline{\text{IN-65}}$ = 1 if input buffer empty	9
$\overline{\text{OUT-32}}$ = 1 if out put buffer empty	10
IP = 1 if IP flag set	11
BUSY = 1 if IN-MODE set and no data available or if OUT-MODE set and no room for next data word	12
RT = 1 if RT flag set	13
unassigned	14
DACT = 1 if 6000 channel de-activated and no data available if IN-MODE was set	15

PROGRAMMING (6000 PP Side)

There are three functions which the 6000 PP may issue to the interface. Their format is:

11	10	9	8	7	6	5	4	3	2	1	0
E	E	E	HL	I/S	C_6	C_5	C_4	C_3	C_2	C_1	C_0

Where:
- EEE is the equipment number
- HL is the halt load bit
- I/S is the interrupt/status function bit
- $C_6, C_5, \ldots C_0$ are communication bits

Halt Load Function (HL=1)

The Halt Load Function is signaled, by setting the HL bit to 1. When the interface receives this function it causes the 7/32 to master clear and then to load and execute the program from its loader storage unit (LSU). This is similar to a "deadstart" on the 6500. The steps taken by the PP after issuing the Halt Load Function are dependent upon the LSU program.

Interrupt Function (HL=0, I/S=1)

The Interrupt function is specified by setting HL to 0 and I/S to 1. When this function is received by the interface and no previous interrupt is pending (IP flag is not set), the following occurs:

1. The IP flag is set.
2. The channel is de-activated.
3. Bits C_6, $C_5 \ldots C_0$ are placed in SP bits SP-1 to SP-7.
4. An interrupt is requested on device nnnnnnnl of the 7/32.

When the interrupt is acknowledged by the 7/32 it should issue a read request on device nnnnnnnl. This will supply the contents of the SP-BITS and IP flag to the 7/32 and will then clear the IP flag and SP-BITS in the interface. The form of the data returned by the read is:

IP	C_6	C_5	C_4	C_3	C_2	C_1	C_0

If an interrupt is pending (IP is set) when this function is issued no de-activation will occur until IP is cleared (the 7/32 issues a read). In th case the PP may decide to de-activate the channel (use bit 2^5 in channel num to avoid hangs) in which case the interrupt request is aborted (ignored).

It is good programming practice to monitor the progress of the interrupt function by issuing a status function after each interrupt request. The status function can also be used to see if a previous interrupt request is pending before issuing another interrupt.

Status Function (HL=0, I/S=0)

The Status Function is specified by setting HL to 0 and I/S to 0. After receiving a status function the interface will go into status mode (set the ST-65 flip-flop) and will make the channel inactive. When the channel again becomes active (the PP inputs data) the interface sends one of two 12 bit status words depending on the setting of C_0 when the function was issued. Each time a word is read by the PP and an empty is returned to the interface, the channel will again become full with an updated copy of the selected status word. Sending a DCN to the interface will clear the status mode. The status reply words are as follows:

$C_0=0$

11	10	9	8	7	6	5	4	3	2	1	0
IP	PF	IN MODE	OUT MODE	SP_0	SP_1	SP_2	SP_3	SP_4	SP_5	SP_6	SP_7

Where:		BIT
	IP = IP flag (1 if interrupt pending)	(11)
	PF = 1 if power fail on 7/32	(10)
	IN-MODE = 1 of IN-MODE flag is set	(9)
	OUT-MODE = 1 if OUT=MODE flag is set	(8)
	SP_0-SP_7 = SP bits register	(7-0)

$C_0=1$

11	10	9	8	7	6	5	4	3	2	1	0
	PF	ST 32	RTW	DCN 65	RT	ACK2	ACK	OUT 32	IN 65	MODE2	MODE

Where:		
	undefined	(11)
	PF = 1 if power fail on 7/32	(10)
	ST-32 = 1 if 7/32 is in general status mode	(9)
	RTW = 1 if 7/32 data interrupt pending	(8)
	DCN-65 = 1 if 6000 sent DCN	(7)
	RT = 1 if RT flag set	(6)
	ACK2 = 1 if IP interrupt acknowledged	(5)
	ACK = 1 RT (data) interrupt acknowledged	(4)
	OUT-32 = OUT-32 flag	(3)
	IN-65 = IN-65 flag	(2)
	MODE2 = MODE2 flag	(1)
	MODE = MODE flag	(0)

PROGRAMMING (7/32 Side)

The interface appears as two separate devices to the 7/32. Thus there are two devices to program and each is significantly different.

Device nnnnnnn0

This device handles all data transfers and controls the format of data transfer used. The following instructions are allowed:

1) Command (OC or OCR)

The command instruction causes the interface to change its mode of operation. The bit assignment for the command instruction are as follows:

8	9	10	11	12	13	14	15
	DCN	ST 32	IN MODE	OUT MODE	RT	MODE2	MODE

where:		BIT
	unassigned	(8)
	DCN = 1 if to send DCN to PP	(9)
	ST-32 = 1 to set status mode, 0 to clear	(10)
	IN-MODE = 1 to set IN=MODE, 0 to clear	(11)
	OUT-MODE = 1 to set OUT-MODE, 0 to clear	(12)
	RT = 1 to set RT MODE, 0 to clear	(13)
	MODE2 = 1 to set MODE2, 0 to clear	(14)
	MODE = 1 to set MODE, 0 to clear	(15)

If both bits 11 and 12 are set only bits 9 and 10 have meaning. For a description of each of the 'mode' flags and their meanings, see the DATA TRANSFER section.

2) Status (SS or SSR)

The Status instruction reads an 8 bit status from the interface. This instruction may be used at any time. The status bits returned are as follows:

8	9	10	11	12	13	14	15
$\overline{\text{ACT-65}}$	$\overline{\text{IN-65}}$	$\overline{\text{OUT-32}}$	IP	BUSY	RT		DACT

Where:		BIT
	$\overline{\text{ACT-65}}$ = 1 if 6000 channel not active	(8)
	$\overline{\text{IN-65}}$ = 1 if input buffer empty	(9)
	$\overline{\text{OUT-32}}$ = 1 if output buffer empty	(10)
	IP = 1 if IP flag set	(11)
	BUSY = 1 if IN-MODE set and no data available or if OUT-MODE set and no room for next data word	(12)
	RT = 1 if RT flag set	(13)
	unassigned	(14)
	DACT = 1 if 6000 channel de-activated and no data available if IN-MODE was set	(15)

3) Read Byte (s) (RD, RDR, RB, RBR, AL, DMA access)

Read data in byte mode, the instruction should only be used when IN-MODE and IN-65 are set and MODE2 and ST-32 are clear, otherwise the 7/32 will time out. (V

4) Read Halfword (RH, RHR, DMA access)

Read a halfword of data. These instructions should only be used when IN-MODE, IN-65, and MODE2 are set. Otherwise, the 7/32 will time out. If ST-32 is set when the read is issued 16 bits of general status is returned instead of data (see DATA TRANSFER sectio

5) Write Byte (s) (WD, WDR, WB, WBR, DMA access)

Send data in byte mode. These instructions should only be used when OUT-MODE is set and OUT-32 and MODE2 are clear. Otherwise, the 7/32 will time out.

6) Write Halfword (WH, WHR, DMA access)

Send a halfword of data. These instruction should only be used when OUT-MODE and MODE2 are set and OUT-32 is clear. Otherwise, the 7/32 will time out.

Device nnnnnnnl

This device handles all interrupts from the interface caused by PP functions. When an interrupt occurs from this device a byte type read should be done. This reads up the IP flag the SP-bits as follows.

IP	SP_1	SP_2	SP_3	SP_4	SP_5	SP_6	SP_7

The IP flag and SP-BIT register in the interface are cleared by the read.

The command instruction (OC, OCR) can be used to place 8 bits of data in the SP-bits register as long as IP is not set. These bits can then be examined by the PP through the PP status function.

The status and write instructions are not defined for this device.

Function

The following is a list of the allowable functions which may be sent to the FEI by a PPU.

SELECT 2400 010 100 XXXXXX* (SEL)

Connect the FEI to the 6000 channel. Once this function is issued the connection remains in effect until a DESELECT is issued. While selected no functions or data received by the FEI will be passed on to other 6000 devices which are connected past this device on the channel daisy chain.

DESELECT 2410 010 100 YYYYYY* (DES)

Disconnect the FEI from the 6000 channel thereby allowing the pass-on network to function in the normal CDC manner.

The two functions described above are similar to the way a CDC 6684 operates.

*These six bits are strapable to any combination of 0's and 1's but XXXXXX must differ in exactly 1 bit position from YYYYYY.

ADDRESS UPPER 001 000 000 WWW (SAU) 1000

This function sets the upper 3 bits (WWW) of the 19 bit address from which the first read or write will take place.

ADDRSS MIDDLE ~~011~~ 001 1WWWWWWWW (SAL) 1400

The function sets - bits 2^8 2^{15} (W's) of the 19 bit address from which the first read or write will take place.

HALT LOAD 011 ~~0~~1dddddddd d = don't care (HL) 3000

Cause the 7/32 to initialize and then read up to 16 bytes of data from device 5 on the multiplexer bus.

INTERRUPT 011 ~~1~~0dddddddd d = don't care (INT) 3400

Causes an interrupt from device 5 on the Interdata multiplexer bus.

LOAD PROGRAM 110 dddddddd d = don't care (LP) 6000

Prepare to accept 8 bit bytes of data from the PPU which will be placed in a 16 byte memory starting at location 0. This memory is used by the 7/32 whenever it attempts to read from device 5.

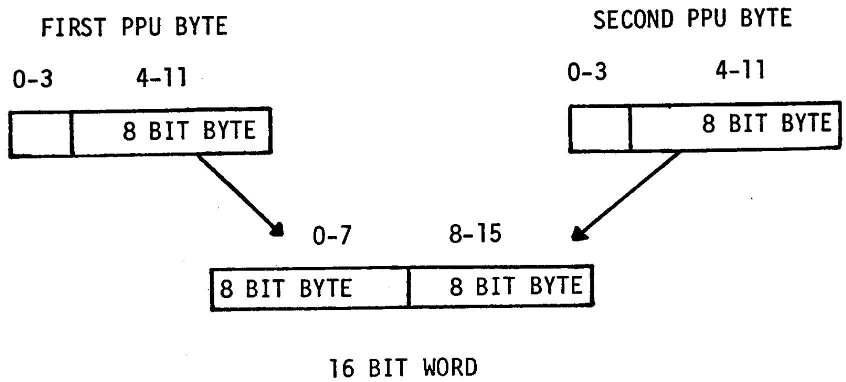
Modes

There are two modes for date transfer, MODE0 nad MODE 1.

MODE 1

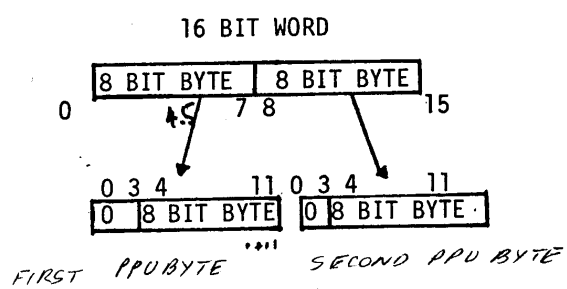
1) WRITE - data from the PPU to the 7/32.

Two consecutive 12 bit bytes are used to create a single 16 bit word to be stored in the 7/32 memory. Only the bottom 8 bits of each 12 bit PPU byte is utilized. The 8 bit byte devised from the first PPU byte is always placed in bits 0-7 of the 16 bit word. The next 8 bit byte derived is always stored in bits 8-15 of the 16 bit word. If after receiving the first 8 bit byte a DCN is received the lower 8 bits (8-15) will be set to 0.



2) READ - data from the 7/32 to a PPU

Each 16 bit word from Interdata memory is divided into two 8 bit bytes. Each byte is packed into the lower 8 bits (4-11) of a 12 bit PPU byte and sent to the PPU. The top 8 bit byte (bits 0-7) is always sent first followed by the lower byte (bits 8-15).

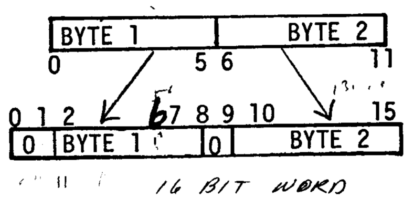


Mode 0

1) WRITE - data from the PPU to the 7/32

A 12 bit PPU word is considered to contain two 6 bit bytes. Byte 1 is bits 0-5, byte 2 is bits 6-11. These two 6 bit bytes are placed in 8 bit bytes of a 16 bit word with the undefined bits (0-1 and 8-9) being set to 0.

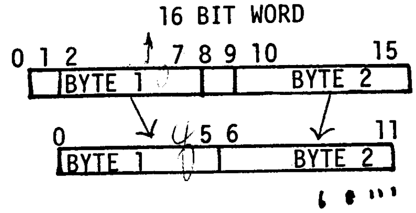
PPU BYTE



2) READ - data from the 7/32 to the PPU

A 16 bit word from Interdata memory is assumed to contain two 6 bit bytes as sub-bytes of its normal 8 bit bytes. These two 6 bit bytes are packed into one 12 bit PPU byte.

16 BIT WORD



PPU BYTE

The following functions are MODE dependent. In each case the mode is determined by the value of M. The value of aaaaaaaa* is used as the lower (bits 2^7 - 2^0) 8 bits of the address from which the first read or write will take place.

READ 100 Maaaaaaaa (RM) 4400

When this function is issued the FEI begins reading data from the 7/32 memory. Each time a word is read from memory the address is incremented by 1. Since there are two 16 bit buffers in the FEI, the interface will almost always be two words ahead of the channel. When the channel becomes active consecutive bytes of data (depending on mode) will be transmitted to the PPU. When the PPU sends a DCN to the FEI all data transmission will halt and the current function (READ) will be cleared. Any data left in the interface will be lost.

* NOTE ALL ADDRESS VALUES ARE HALF WORD ADDRESSES

If an error condition (parity error or read from non-existant memory) should arise this information will move with the corresponding data through the FEI. If the PPU attempts to read the bogus data (accepts it by sending an empty reply) the FEI will DCN the channel when it receives the empty signal. In this case the current function is not cleared and the type of error can be found by doing a STATUS function (see status). Issuing any other function will clear the error condition and resume normal operation.

READ AND SET   101 daaaaaaaa   d = don't care (RSM) 5

This function prepares the FEI to do a test and set type read from a single location in the 7/32 common memory. The MODE is always forced to 1 so that exactly 2 bytes of data will be received by the PPU. After the second byte has been received the channel remains empty until the transfer is terminated by the PPU with a DCN. Note that the address register is not changed by this function.

WRITE   111 Maaaaaaaa   (WM)   7400

This function allows the PPU to write data into the 7/32 memory. When the channel becomes full the FEI will accept the data and return an empty to the channel. This process will continue until the PPU sends DCN or an error has occured. The only error that can occur on a write is a reference to a ~~non-existant memory~~ location. When this happens the FEI will DCN the channel and set the corresponding status bit. Since the FEI double buffers the data an unhangable DCN instruction should be used to protect against channel hangs.

STATUS   0000 dddddddd   d = don't care (ST)   0000

This function allows the reading of status information by the PPU. When the channel becomes active the 12 bit status byte is sent to the PPU. Each time the PPU accepts a status byte a new updated status byte is sent to the PPU. The process is terminated when the PPU DCN's the channel.

0	1	2	3	4	5	6	7	8	9	10	11
A	B	C	D	E	F	G	H	I	U	U	U
1	0	0	1	1	1	0	0	0	1	1	1

STATUS BYTE

Where:

A = set to 1 whenever the 7/32 is initialized
B = set to 1 when an attempt is made to write to a non-existant memory location in the 7/32
CD = a two bit status detailing the condition of the last byte accepted by the PPU on a read.

00 no error data is valid
01 parity error
10 memory malfunction
11 read from non-existant

E = value of the mode bit when error occured
F = set to 1 if a read was in progress ~~ehn~~ when an error occured
G = set to 1 if a write was in progress ~~ehn~~ when an error occured
H = a Halt Load function is in progress
I = an Interrupt request is pending
U = undefined at this time

<u>CLEAR INITIALIZE</u> 0001 dddddddd d = don't care

This function allows the PPU to clear the Initialize flag in the status register.

SOCKET	ADDRESS	TYPE	SUBSYS PRT: INT:	PHONE	BAUD RATE	I/O ORD NOLOGIN	ROUTE IOTERM	TERMINAL	RESTRICTIONS	CONN/COMMENTS
1	002	TTY	INT	-	AUTO	YES	YES	CRT		7/32 CONSOLE
--------	006	BUS A	------							
2	030	PALLS	INT	-	AUTO		YES			A-00 OPERATOR TTY
3	0A0	CMUX 2	INT	-	4800					C-00 BIU HSTC00
4	0A2	CMUX 2	INT	-	4800					C-01 BIU HSTC01
5	0A4	CMUX 2	INT	-	4800					C-02 BIU HSTC02
6	0A6	CMUX 2	INT	-	4800					C-03 BIU HSTC03
7	0A8	CMUX 2	INT	-	4800					C-04 BIU HSTC04
8	0AA	CMUX 2	INT	-	4800					C-05 BIU HSTC05
9	0AC	CMUX 2	INT	-	4800					C-06 BIU HSTC06
10	0AE	CMUX	INT	-	AUTO					C-07 BAD
11	0B0	CMUX 2	INT	-	4800					C-09 BIU HSTC09
12	0B2	CMUX 2	INT	-	4800					C-08 BIU HSTC08
13	0B4	CMUX 2	INT	-	4800					C-11 BIU HSTC11
14	0B6	CMUX 2	INT	-	4800					C-10 BIU HSTC10
15	0B8	CMUX 2	INT	-	4800					C-13 ~~BIU HSTC13~~
16	0BA	CMUX 2	INT	-	4800					C-12 BIU HSTC12 (not C07).
17	0BC	CMUX 2	INT	-	4800					C-15 ~~BIU HSTC15~~
18	0C0	CMUX 2	INT	-	4800					C-16 IBMPC 110-1
19	0C2	CMUX 2	INT	-	4800					C-17 IBMPC 110-2
20	0C4	CMUX 2	INT	-	4800					C-18 IBMPC 110-3
21	0C6	CMUX 2	INT	-	4800					C-19 IBMPC 110-4
22	0C8	CMUX 2	INT	-	4800					C-20 IBMPC 110-5
23	0CA	CMUX 2	INT	-	4800					C-21 IBMPC 110-6
24	0CC	CMUX 2	INT	-	4800					C-22 IBMPC 110-7
25	0CE	CMUX 2	INT	-	4800					C-23 IBMPC 110-8
26	0D0	CMUX 2	INT	-	4800					C-24 IBMPC 110-9
27	0D2	CMUX 2	INT	-	4800					C-25 IBMPC 110-10
28	0D4	CMUX 2	INT	-	4800					C-26 IBMPC 110-11
29	0D6	CMUX 2	INT	-	4800					C-27 IBMPC 110-12
30	0D8	CMUX 2	INT	-	4800					C-28 IBMPC 110-13
31	0DA	CMUX 2	INT	-	4800					C-29 IBMPC 110-14
32	0DC	CMUX 2	INT	-	4800					C-30 IBMPC 110-15
33	0DE	CMUX 2	INT	-	4800					C-31 IBMPC 110-16
34	0E0	CMUX 2	INT	-	AUTO-4800					B-24 515-4
35	0E2	CMUX 2	INT	-	AUTO-4800					B-25 220
36	0E4	CMUX 2	INT	-	AUTO-4800					B-26 502-1 KEYPUNCH
37	0E6	CMUX 2	INT	-	AUTO-4800					B-27 SPARE
38	0E8	CMUX 2	INT	-	AUTO-4800					B-28 ~~SPARE~~
39	0EA	CMUX 2	INT	-	AUTO-4800					B-29 SPARE
40	0EC	CMUX 2	INT	-	AUTO-4800					B-30 SPARE
41	0EE	CMUX 2	INT	-	AUTO-4800					B-31 SPARE
42	0F0	CMUX 2	INT	-	AUTO-4800					B-32 SPARE
43	0F2	CMUX 2	INT	-	AUTO-4800					B-33 SPARE
44	0F4	CMUX 2	INT	-	AUTO-4800					B-34 SPARE
45	0F6	CMUX 2	INT	-	AUTO-4800					B-35 SPARE
46	0F8	CMUX 2	INT	-	4800					B-36 BIU HSTB36
47	0FA	CMUX 2	INT	-	4800					B-37 BIU HSTB37
48	0FC	CMUX 2	INT	-	4800					B-38 BIU HSTB38
49	0FE	CMUX 2	INT	-	4800					B-39 BIU HSTB39
50	032	PALLS	INT	353-8500	AUTO					A-01 353-8500 1A1
51	034	PALLS	INT	353-8502	AUTO					A-02 353-8502 1A2
52	036	PALLS	INT	353-8504	AUTO					A-03 353-8504 1A3
53	038	PALLS	INT	353-8506	AUTO					A-04 353-8506 1A4
54	03A	PALLS	INT	353-8508	AUTO					A-05 353-8508 1A5
55	03C	PALLS	INT	353-8510	AUTO					A-06 353-8510 1A6
56	03E	PALLS	INT	353-8512	AUTO					A-07 353-8512 1A7
57	040	PALLS	INT	353-8514	AUTO					A-08 353-8514 1A8
58	042	PALLS	INT	353-8516	AUTO					A-09 353-8516 1A9
59	044	PALLS	INT	353-8518	AUTO					A-10 353-8518 1A10
60	046	PALLS	INT	353-8520	AUTO					A-11 353-8520 1A11

FRONT-END DEVICES

SOCKET	ADDRESS	TYPE	SUBSYS PRT: INT:	PHONE	BAUD RATE	I/O ORD NOLOGIN	ROUTE IOTERM	TERMINAL	RESTRICTIONS	CONN/COMMENTS
61	048	PALLS	INT	353-8522	AUTO					A-12 353-8522 1A12
62	04A	PALLS	INT	353-8524	AUTO					A-13 353-8524 ~~1A13~~
63	04C	PALLS	INT	353-8526	AUTO					A-14 353-8526 1A14
64	04E	PALLS	INT	353-8528	AUTO					A-15 353-8528 1A15 bad
65	050	PALLS	INT	353-8530	AUTO					A-16 353-8530 1A16
66	052	PALLS	INT	353-8532	AUTO					A-17 353-8532 1B1
67	054	PALLS	INT	353-8550	AUTO					A-18 353-8550 1B2
68	056	PALLS	INT	353-8552	AUTO					A-19 353-8552 1B3
69	058	PALLS	INT	353-8554	AUTO					A-20 353-8554 1B4
70	05A	PALLS	INT	353-8556	AUTO					A-21 353-8556 1B5
~~71~~	05C	PALLS	INT	353-8558	~~AUTO~~					A-22 353-8558 1B6
72	05E	PALLS	INT	-	AUTO-4800				38558	~~A-23 SPARE~~ 38560 ?
73	060	PALLS	INT	353-8562	AUTO					A-24 353-8562 1B8
74	062	PALLS	INT	353-8564	AUTO					A-25 353-8564 1B9
75	064	PALLS	INT	353-8566	AUTO					A-26 353-8566 1B10
76	066	PALLS	INT	353-8567	AUTO					A-27 353-8567 1B12
77	068	PALLS	INT	353-8570	AUTO					A-28 353-8570 2A1
78	06A	PALLS	INT	353-8572	AUTO					A-29 353-8572 2A5
79	06C	PALLS	INT	353-8574	AUTO					A-30 353-8574 2A9
80	06E	PALLS	INT	353-8576	AUTO					A-31 353-8576 2A13
81	070	PALLS	INT	353-8578	AUTO					B-00 353-8578 2B1
82	072	PALLS	INT	353-8580	AUTO					B-01 353-8580 2B5
83	074	PALLS	INT	353-8582	AUTO					B-02 353-8582 2B9
84	076	PALLS	INT	353-8584	AUTO					B-03 353-8584 2B13
85	078	PALLS	INT	-	AUTO				38516	B-04 SPARE
86	07A	PALLS	INT	-	AUTO-4800					✓ B-05 SPARE
87	07C	PALLS	INT	353-8585	~~AUTO~~					B-06 353-8585 2B15
88	07E	PALLS	INT	353-8586	AUTO					B-07 353-8586 2C1
89	080	PALLS	INT	353-8587	AUTO					B-08 353-8587 2C3
90	082	PALLS	INT	353-8588	AUTO					B-09 353-8588 2C5
91	084	PALLS	INT	353-8599	AUTO					B-10 353-8599 2D7
92	086	PALLS	INT	-	AUTO					B-11 SPARE
93	088	PALLS	INT	-	AUTO					B-12 508 DIGITIZER
94	08A	PALLS	INT	-	AUTO					B-13 ~~SPARE~~
95	08C	PALLS	INT	353-8560	AUTO				38556	B-14 353-8560 1B7
96	08E	PALLS	INT	-	AUTO-4800					B-15 ~~SPARE~~
97	090	PALLS	INT	353-8594	AUTO					B-16 353-8594 2D9
98	092	PALLS	INT	-	AUTO					B-17 BAD
99	094	PALLS	INT	353-8596	AUTO					B-18 353-8596 4B15
100	096	PALLS	INT	353-8597	AUTO					B-19 353-8597 1B15
101	098	PALLS	INT	353-8598	AUTO					B-20 353-8598 1B16
102	09A	PALLS	INT	353-8595	AUTO					B-21 353-8595 2D11
103	09C	PALLS	INT	353-8568	AUTO					B-22 353-8568 1B13
104	09E	PALLS	INT	353-8569	AUTO					B-23 353-8569 1B14
--------	007	BUS B	----------							
105	1A0	CMUX 2	INT	-	AUTO-4800					G-00 208 TAPE LIB
106	1A2	CMUX 2	INT	-	4800					G-01 110-17 (FRONT)
107	1A4	CMUX 2	INT	-	AUTO-4800					G-02 SPARE
108	1A6	CMUX 2	INT	-	AUTO-4800					G-03 515-2
109	1A8	CMUX 2	INT	-	9600					G-04 COMNET PDP 11/70
110	1AA	CMUX 2	INT	-	AUTO-4800					G-05 AG ECON 306-1
111	1AC	CMUX 2	INT	-	AUTO-4800					G-06 ~~AG ECON 306-2~~ bad
112	1AE	CMUX 2	INT	-	AUTO-4800					G-07 505-1

SOCKET	ADDRESS	TYPE	SUBSYS PRT: INT:	PHONE	BAUD RATE	I/O ORD NOLOGIN	ROUTE IOTERM	TERMINAL	RESTRICTIONS	CONN/COMMENTS
113	1B0	CMUX	INT	-	AUTO					G-08 BAD 3/24/82 TDC
114	1B2	CMUX 2	INT	-	AUTO-4800					G-09 SPARE
115	1B4	CMUX 2	INT	-	AUTO-4800					G-10 SPARE
116	1B6	CMUX	INT	353-8589	AUTO					G-11 353-8589 2C7
117	1B8	CMUX	INT	353-8590	AUTO					G-12 353-8590 2C9
118	1BA	CMUX	INT	353-8591	AUTO					G-13 353-8591 2C11
119	1BC	CMUX	INT	353-8592	AUTO					G-14 353-8592 2C13
120	1BE	CMUX	INT	353-8593	AUTO					G-15 353-8593 2C15
121	1C0	CMUX 2	INT	-	4800					G-16 BIU HSTG16
122	1C2	CMUX 2	INT	-	4800					G-17 BIU HSTG17
123	1C4	CMUX 2	INT	-	4800					G-18 BIU HSTG18
124	1C6	CMUX 2	INT	-	4800					G-19 BIU HSTG19
125	1C8	CMUX 2	INT	-	4800					G-20 BIU HSTG20
126	1CA	CMUX 2	INT	-	4800					G-21 BIU HSTG21
127	1CC	CMUX 2	INT	-	4800					G-22 BIU HSTG22
128	1CE	CMUX 2	INT	-	4800					G-23 BIU HSTG23
129	130	PALLS	INT	-	AUTO					D-00 BUSY OUT SWITCH
130	132	PALLS	INT	353-8501	AUTO					D-01 353-8501 3A1
131	134	PALLS	INT	353-8503	AUTO					D-02 353-8503 3A2
132	136	PALLS	INT	353-8505	AUTO					D-03 353-8505 3A3
133	138	PALLS	INT	353-8507	AUTO					D-04 353-8507 3A4
134	13A	PALLS	INT	353-8509	AUTO					D-05 353-8509 3A5
135	13C	PALLS	INT	353-8511	AUTO					D-06 353-8511 3A6
136	13E	PALLS	INT	353-8513	AUTO					D-07 353-8513 3A7
137	140	PALLS	INT	-	AUTO					D-08 BAD
138	142	PALLS	INT	353-8517	AUTO					D-09 353-8517 3A9
139	144	PALLS	INT	-	AUTO					D-10 BAD
140	146	PALLS	INT	353-8521	AUTO					D-11 353-8521 3A11
141	148	PALLS	INT	353-8523	AUTO					D-12 353-8523 3A12
142	14A	PALLS	INT	353-8525	AUTO					D-13 353-8525 3A13
143	14C	PALLS	INT	353-8527	AUTO					D-14 353-8527 3A14
144	14E	PALLS	INT	353-8529	AUTO					D-15 353-8529 3A15
145	150	PALLS	INT	353-8531	AUTO					D-16 353-8531 3A16
146	152	PALLS	INT	353-8533	AUTO					D-17 353-8533 3B1
147	154	PALLS	INT	353-8551	AUTO					D-18 353-8551 3B2
148	156	PALLS	INT	353-8553	AUTO					D-19 353-8553 3B3
149	158	PALLS	INT	353-8555	AUTO					D-20 353-8555 3B4
150	15A	PALLS	INT	353-8557	AUTO					D-21 353-8557 3B5
151	15C	PALLS	INT	353-8559	AUTO					D-22 353-8559 3B6
152	15E	PALLS	INT	353-8561	AUTO					D-23 353-8561 3B7
153	160	PALLS	INT	353-8563	AUTO					D-24 353-8563 3B8
154	162	PALLS	INT	353-8565	AUTO					D-25 353-8565 3B9
155	164	PALLS	INT	353-8515	AUTO					D-26 353-8515 3A8
156	166	PALLS	INT	-	AUTO-4800					D-27 SPARE
157	168	PALLS	INT	353-8571	AUTO					E-00 353-8571 2A3
158	16A	PALLS	INT	353-8573	AUTO					E-01 353-8573 2A7
159	16C	PALLS	INT	353-8575	AUTO					E-02 353-8575 2A11
160	16E	PALLS	INT	353-8577	AUTO					E-03 353-8577 2A15
161	170	PALLS	INT	353-8579	AUTO					E-04 353-8579 2B3
162	172	PALLS	INT	353-8581	AUTO					E-05 353-8581 2B7
163	174	PALLS	INT	353-8583	AUTO					E-06 353-8583 2B11
164	176	PALLS	INT	-	AUTO					E-07 STATUS DISPLAY
165	178	PALLS	INT	353-8519	AUTO					E-08 353-8519 3A10
166	17A	PALLS	INT	-	AUTO					E-09 SPARE
167	17C	PALLS	INT	-	AUTO					E-10 SPARE
168	17E	PALLS	INT	-	AUTO					E-11 SPARE
169	180	PALLS	INT	-	AUTO					E-12 212-E4 PT10
170	182	PALLS	INT	-	AUTO					E-13 212-E3 PT9
171	184	PALLS	INT	-	AUTO					E-14 212-E2 PT8
172	186	PALLS	INT	-	AUTO					E-15 212-E1 PT7

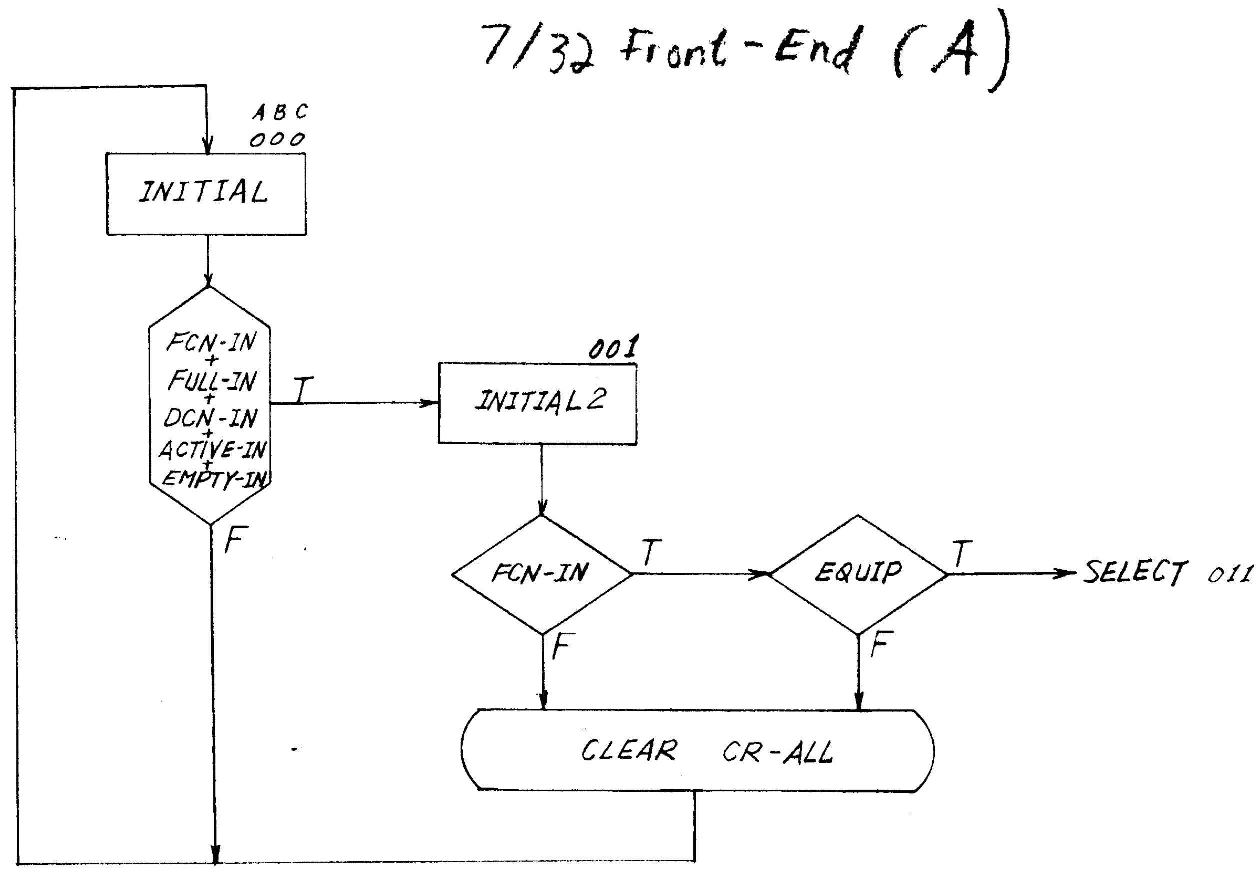
SOCKET	ADDRESS	TYPE	SUBSYS PRT: INT:	PHONE	BAUD RATE	I/O ORD NOLOGIN	ROUTE IOTERM	TERMINAL	RESTRICTIONS	CONN/COMMENTS
173	188	PALLS	INT	-	AUTO					E-16 210-A9 PT2
174	18A	PALLS	INT	-	AUTO					E-17 210-A2 PT5
175	18C	PALLS	INT	-	AUTO					E-18 210-A1 PT4
176	18E	PALLS	INT	-	AUTO					E-19 210-A7 PT6
177	190	PALLS	INT	-	AUTO					E-20 SPARE
178	192	PALLS	INT	-	AUTO					E-21 SPARE
179	194	PALLS	INT	-	AUTO					E-22 SPARE
180	196	PALLS	INT	-	AUTO					E-23 SPARE
181	198	PALLS	INT	-	AUTO					E-24 210-A10 PT3
182	19A	PALLS	INT	-	AUTO					E-25 210-A8 PT1
183	19C	PALLS	INT	-	AUTO					E-26 SPARE
184	19E	PALLS	INT	-	AUTO	YES	YES			E-27 I/O TERMINAL
185	1E6	PR96	PRT	-	AUTO	80	B			PRINTER PAF80
186	1E8	PR64	PRT	-	AUTO	81	B			PRINTER PAU81
187	1EA	PR64	PRT	-	AUTO	82	A			PRINTER PAU82
188	1EC	PR96	PRT	-	AUTO	83	C			PRINTER PAF83
--------	008	BUS C	----------							
189	2B0	CMUX 2	INT	-	AUTO					F-09 ENG 504-1
190	2B2	CMUX 2	INT	-	AUTO					F-08 ENG 504-2
191	2B4	CMUX 2	INT	-	AUTO-4800					F-11 SYS 301-4
192	2B6	CMUX 2	INT	-	4800					F-10 BIU HSTF10
193	2B8	CMUX 2	INT	-	4800					F-13 BIU HSTF13
194	2BA	CMUX 2	INT	-	4800					F-12 BIU HSTF12
195	2BC	CMUX 2	INT	-	4800					F-15 BIU HSTF15
196	2BE	CMUX 2	INT	-	4800					F-14 BIU HSTF14
197	2C0	CMUX 2	INT	-	4800					F-17 BIU HSTF17
198	2C2	CMUX 2	INT	-	4800					F-16 BIU HSTF16
199	2C4	CMUX 2	INT	-	4800					F-19 BIU HSTF19
200	2C6	CMUX 2	INT	-	4800					F-18 BIU HSTF18
201	2C8	CMUX 2	INT	-	4800					F-21 BIU HSTF21
202	2CA	CMUX 2	INT	-	4800					F-20 BIU HSTF20
203	2CC	CMUX 2	INT	-	4800					F-23 BIU HSTF23
204	2CE	CMUX 2	INT	-	4800					F-22 BIU HSTF22
205	2D0	CMUX 2	INT	-	4800					F-25 BIU HSTF25
206	2D2	CMUX 2	INT	-	4800					F-24 BIU HSTF24
207	2D4	CMUX 2	INT	-	4800					F-27 BIU HSTF27
208	2D6	CMUX 2	INT	-	4800					F-26 BIU HSTF26
209	2D8	CMUX 2	INT	-	4800					F-29 BIU HSTF29
210	2DA	CMUX	INT	-	AUTO					F-28 BAD
211	2DC	CMUX 2	INT	-	4800					F-31 BIU HSTF31
212	2DE	CMUX 2	INT	-	4800					F-30 BIU HSTF30
--------	009	BUS D	----------							
213	330	PALLS	INT	-	4800					I-00 212-A1
214	332	PALLS	INT	-	4800					I-01 212-A2
215	334	PALLS	INT	-	4800					I-02 212-A3
216	336	PALLS	INT	-	4800					I-03 212-A4
217	338	PALLS	INT	-	4800					I-04 212-A5
218	33A	PALLS	INT	-	4800					I-05 212-A6
219	33C	PALLS	INT	-	4800					I-06 212-A7
220	33E	PALLS	INT	-	4800					I-07 212-A8
221	340	PALLS	INT	-	4800					I-08 212-B1
222	342	PALLS	INT	-	4800					I-09 212-B2
223	344	PALLS	INT	-	4800					I-10 212-B3
224	346	PALLS	INT	-	4800					I-11 212-B4
225	348	PALLS	INT	-	4800					I-12 212-B5
226	34A	PALLS	INT	-	4800					I-13 212-B6
227	34C	PALLS	INT	-	4800					I-14 212-B7
228	34E	PALLS	INT	-	4800					I-15 212-B8

SOCKET	ADDRESS	TYPE	SUBSYS PRT: INT:	PHONE	BAUD RATE	I/O ORD NOLOGIN	ROUTE IOTERM	TERMINAL	RESTRICTIONS	CONN/COMMENTS
229	350	PALLS	INT	-	4800					I-16 212-C1
230	352	PALLS	INT	-	4800					I-17 212-C2
231	354	PALLS	INT	-	4800					I-18 212-C3
232	356	PALLS	INT	-	4800					I-19 212-C4
233	358	PALLS	INT	-	4800					I-20 212-C5
234	35A	PALLS	INT	-	4800					I-21 212-C6
235	35C	PALLS	INT	-	4800					I-22 212-C7
236	35E	PALLS	INT	-	4800					I-23 212-C8
237	3A0	CMUX 2	INT	-	4800					H-00 212-E5 HANDICAP
238	3A2	CMUX 2	INT	-	4800					H-01 212-E6
239	3A4	CMUX 2	INT	-	4800					H-02 212-E7
240	3A6	CMUX 2	INT	-	4800					H-03 212-E8
241	3A8	CMUX 2	INT	-	4800					H-04 212-D1
242	3AA	CMUX 2	INT	-	4800					H-05 212-D6
243	3AC	CMUX 2	INT	-	4800					H-06 212-D7
244	3AE	CMUX 2	INT	-	4800					H-07 BAD
245	3B0	CMUX 2	INT	-	4800					H-08 BAD
246	3B2	CMUX 2	INT	-	4800					H-09 212-D2
247	3B4	CMUX 2	INT	-	4800					H-10 212-D3
248	3B6	CMUX 2	INT	-	4800					H-11 212-D4
249	3B8	CMUX 2	INT	-	4800					H-12 SPARE
250	3BA	CMUX 2	INT	-	4800					H-13 SPARE
251	3BC	CMUX 2	INT	-	4800					H-14 SPARE
252	3BE	CMUX 2	INT	-	4800					H-15 SPARE
253	3C0	CMUX 2	INT	-	4800					I-24 BIU HSTI24
254	3C2	CMUX 2	INT	-	4800					I-25 BIU HSTI25
255	3C4	CMUX 2	INT	-	4800					I-26 BIU HSTI26
256	3C6	CMUX 2	INT	-	4800					I-27 BIU HSTI27
257	3C8	CMUX 2	INT	-	4800					I-28 BIU HSTI28
258	3CA	CMUX 2	INT	-	4800					I-29 BIU HSTI29
259	3CC	CMUX 2	INT	-	4800					I-30 BIU HSTI30
260	3CE	CMUX 2	INT	-	4800					I-31 BIU HSTI31
261	3D0	CMUX 2	INT	-	4800					J-00 BIU HSTJ00
262	3D2	CMUX 2	INT	-	4800					J-01 BIU HSTJ01
263	3D4	CMUX 2	INT	-	4800					J-02 BIU HSTJ02
264	3D6	CMUX 2	INT	-	4800					J-03 BIU HSTJ03
265	3D8	CMUX 2	INT	-	4800					J-04 BIU HSTJ04
266	3DA	CMUX 2	INT	-	4800					J-05 BIU HSTJ05
267	3DC	CMUX 2	INT	-	4800					J-06 BIU HSTJ06
268	3DE	CMUX 2	INT	-	4800					J-07 BIU HSTJ07
269	3E0	CMUX 2	INT	-	4800					J-08 BIU HSTJ08
270	3E2	CMUX 2	INT	-	4800					J-09 BIU HSTJ09
271	3E4	CMUX 2	INT	-	4800					J-10 BIU HSTJ10
272	3E6	CMUX 2	INT	-	4800					J-11 BIU HSTJ11
273	3E8	CMUX 2	INT	-	4800					J-12 BIU HSTJ12
274	3EA	CMUX 2	INT	-	4800					J-13 BIU HSTJ13
275	3EC	CMUX 2	INT	-	4800					J-14 BIU HSTJ14
276	3EE	CMUX 2	INT	-	4800					J-15 BIU HSTJ15

SOCKET	ADDRESS	TYPE	SUBSYS PRT: INT:	PHONE	BAUD RATE	I/O ORD NOLOGIN	ROUTE IOTERM	TERMINAL	RESTRICTIONS	CONN/COMMENTS
1	002	TTY	INT	-	AUTO	YES	YES	CRT		7/32 CONSOLE
2	0A0	CMUX 2	INT	-	AUTO		YES			F-01 OPERATOR TTY
3	0A2	CMUX 2	INT	-	4800					F-00 BIU HSTF00(M65)
4	0A4	CMUX 2	INT	-	4800					F-03 BIU HSTF03(M65)
5	0A6	CMUX 2	INT	-	4800					F-02 BIU HSTF02(M65)
6	0A8	CMUX 2	INT	-	4800					F-05 BIU HSTF05(M65)
7	0AA	CMUX 2	INT	-	AUTO					F-04 504-3
8	0AC	CMUX 2	INT	353-0869	AUTO					F-07 353-0869 1C7
--------	006	BUS C								
9	0B0	CMUX 2	INT	-	AUTO					F-09 ENG 504-1
10	0B2	CMUX 2	INT	-	AUTO					F-08 ENG 504-2
11	0B4	CMUX 2	INT	-	AUTO-4800					F-11 SYS 301-4
12	0B6	CMUX 2	INT	-	4800					F-10 BIU HSTF10
13	0B8	CMUX 2	INT	-	4800					F-13 BIU HSTF13
14	0BA	CMUX 2	INT	-	4800					F-12 BIU HSTF12
15	0BC	CMUX 2	INT	-	4800					F-15 BIU HSTF15
16	0BE	CMUX 2	INT	-	4800					F-14 BIU HSTF14
17	0C0	CMUX 2	INT	-	4800					F-17 BIU HSTF17
18	0C2	CMUX 2	INT	-	4800					F-16 BIU HSTF16
19	0C4	CMUX 2	INT	-	4800					F-19 BIU HSTF19
20	0C6	CMUX 2	INT	-	4800					F-18 BIU HSTF18
21	0C8	CMUX 2	INT	-	4800					F-21 BIU HSTF21
22	0CA	CMUX 2	INT	-	4800					F-20 BIU HSTF20
23	0CC	CMUX 2	INT	-	4800					F-23 BIU HSTF23
24	0CE	CMUX 2	INT	-	4800					F-22 BIU HSTF22
25	0D0	CMUX 2	INT	-	4800					F-25 BIU HSTF25
26	0D2	CMUX 2	INT	-	4800					F-24 BIU HSTF24
27	0D4	CMUX 2	INT	-	4800					F-27 BIU HSTF27
28	0D6	CMUX 2	INT	-	4800					F-26 BIU HSTF26
29	0D8	CMUX 2	INT	-	4800					F-29 BIU HSTF29
30	0DA	CMUX	INT	-	AUTO					F-28 BAD
31	0DC	CMUX 2	INT	-	4800					F-31 BIU HSTF31
32	0DE	CMUX 2	INT	-	4800					F-30 BIU HSTF30
--------	009	BUS D								
33	130	PALLS	INT	-	4800					I-00 212-A1
34	132	PALLS	INT	-	4800					I-01 212-A2
35	134	PALLS	INT	-	4800					I-02 212-A3
36	136	PALLS	INT	-	4800					I-03 212-A4
37	138	PALLS	INT	-	4800					I-04 212-A5
38	13A	PALLS	INT	-	4800					I-05 212-A6
39	13C	PALLS	INT	-	4800					I-06 212-A7
40	13E	PALLS	INT	-	4800					I-07 212-A8
41	140	PALLS	INT	-	4800					I-08 212-B1
42	142	PALLS	INT	-	4800					I-09 212-B2
43	144	PALLS	INT	-	4800					I-10 212-B3
44	146	PALLS	INT	-	4800					I-11 212-B4
45	148	PALLS	INT	-	4800					I-12 212-B5
46	14A	PALLS	INT	-	4800					I-13 212-B6
47	14C	PALLS	INT	-	4800					I-14 212-B7
48	14E	PALLS	INT	-	4800					I-15 212-B8
49	150	PALLS	INT	-	4800					I-16 212-C1
50	152	PALLS	INT	-	4800					I-17 212-C2
51	154	PALLS	INT	-	4800					I-18 212-C3
52	156	PALLS	INT	-	4800					I-19 212-C4
53	158	PALLS	INT	-	4800					I-20 212-C5
54	15A	PALLS	INT	-	4800					I-21 212-C6
55	15C	PALLS	INT	-	4800					I-22 212-C7
56	15E	PALLS	INT	-	4800					I-23 212-C8

A BIU was a "Bus Interface Unit"
that provided remote serial links
(via X.25) over the campus
network. /mrr December 2003

SOCKET	ADDRESS	TYPE	SUBSYS PRT: INT:	PHONE	BAUD RATE	I/O ORD NOLOGIN	ROUTE IOTERM	TERMINAL	RESTRICTIONS	CONN/COMMENTS
57	1A0	CMUX 2	INT	-	4800					H-00 212-E5 HANDICAP
58	1A2	CMUX 2	INT	-	4800					H-01 212-E6
59	1A4	CMUX 2	INT	-	4800					H-02 212-E7
60	1A6	CMUX 2	INT	-	4800					H-03 212-E8
61	1A8	CMUX 2	INT	-	4800					H-04 212-D1
62	1AA	CMUX 2	INT	-	4800					H-05 212-D6
63	1AC	CMUX 2	INT	-	4800					H-06 212-D7
64	1AE	CMUX 2	INT	-	4800					H-07 BAD
65	1B0	CMUX 2	INT	-	4800					H-08 BAD
66	1B2	CMUX 2	INT	-	4800					H-09 212-D2
67	1B4	CMUX 2	INT	-	4800					H-10 212-D3
68	1B6	CMUX 2	INT	-	4800					H-11 212-D4
69	1B8	CMUX 2	INT	-	4800					H-12 SPARE
70	1BA	CMUX 2	INT	-	4800					H-13 SPARE
71	1BC	CMUX 2	INT	-	4800					H-14 SPARE
72	1BE	CMUX 2	INT	-	4800					H-15 SPARE
73	1C0	CMUX 2	INT	-	4800					I-24 BIU HSTI24
74	1C2	CMUX 2	INT	-	4800					I-25 BIU HSTI25
75	1C4	CMUX 2	INT	-	4800					I-26 BIU HSTI26
76	1C6	CMUX 2	INT	-	4800					I-27 BIU HSTI27
77	1C8	CMUX 2	INT	-	4800					I-28 BIU HSTI28
78	1CA	CMUX 2	INT	-	4800					I-29 BIU HSTI29
79	1CC	CMUX 2	INT	-	4800					I-30 BIU HSTI30
80	1CE	CMUX 2	INT	-	4800					I-31 BIU HSTI31
81	1D0	CMUX 2	INT	-	4800					J-00 BIU HSTJ00
82	1D2	CMUX 2	INT	-	4800					J-01 BIU HSTJ01
83	1D4	CMUX 2	INT	-	4800					J-02 BIU HSTJ02
84	1D6	CMUX 2	INT	-	4800					J-03 BIU HSTJ03
85	1D8	CMUX 2	INT	-	4800					J-04 BIU HSTJ04
86	1DA	CMUX 2	INT	-	4800					J-05 BIU HSTJ05
87	1DC	CMUX 2	INT	-	4800					J-06 BIU HSTJ06
88	1DE	CMUX 2	INT	-	4800					J-07 BIU HSTJ07
89	1E0	CMUX 2	INT	-	4800					J-08 BIU HSTJ08
90	1E2	CMUX 2	INT	-	4800					J-09 BIU HSTJ09
91	1E4	CMUX 2	INT	-	4800					J-10 BIU HSTJ10
92	1E6	CMUX 2	INT	-	4800					J-11 BIU HSTJ11
93	1E8	CMUX 2	INT	-	4800					J-12 BIU HSTJ12
94	1EA	CMUX 2	INT	-	4800					J-13 BIU HSTJ13
95	1EC	CMUX 2	INT	-	4800					J-14 BIU HSTJ14
96	1EE	CMUX 2	INT	-	4800					J-15 BIU HSTJ15

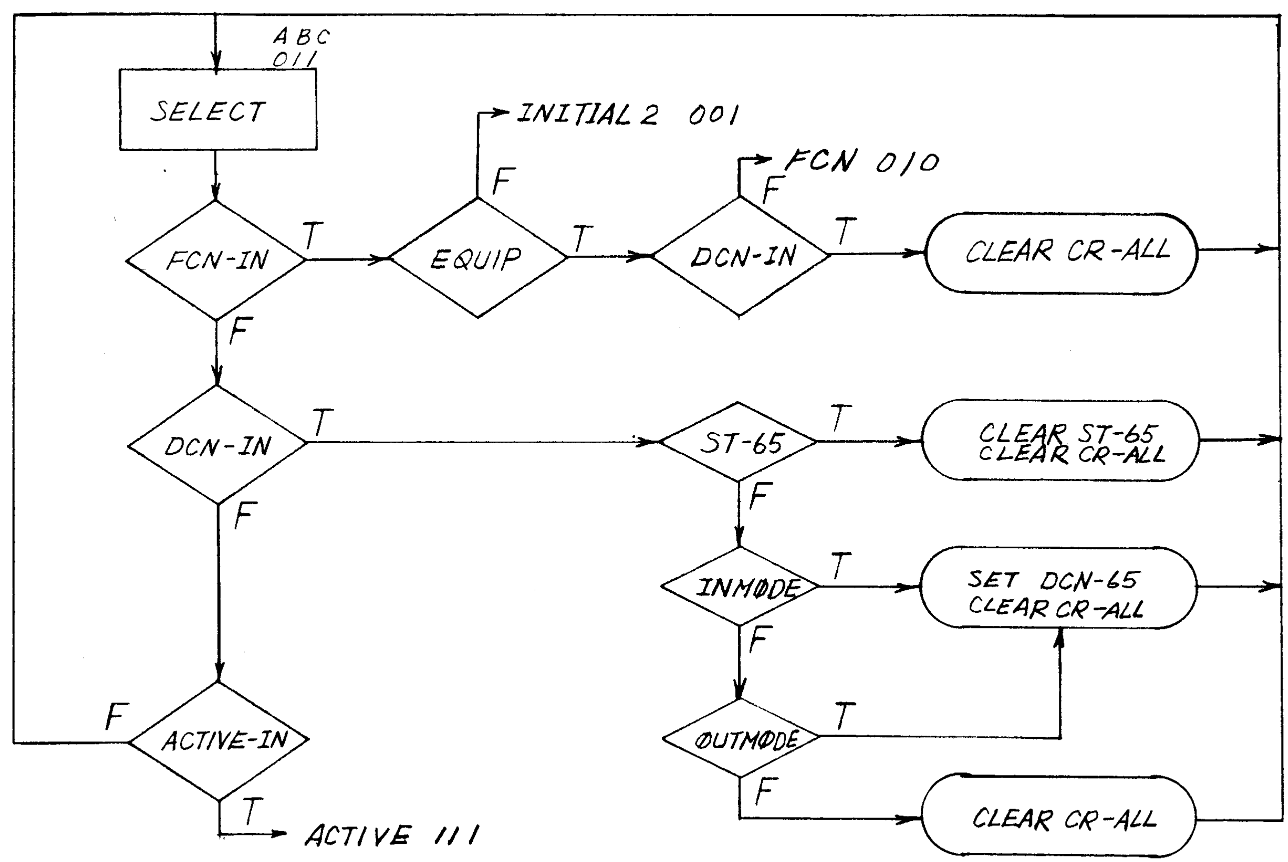


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— M65-1 INITIAL

1

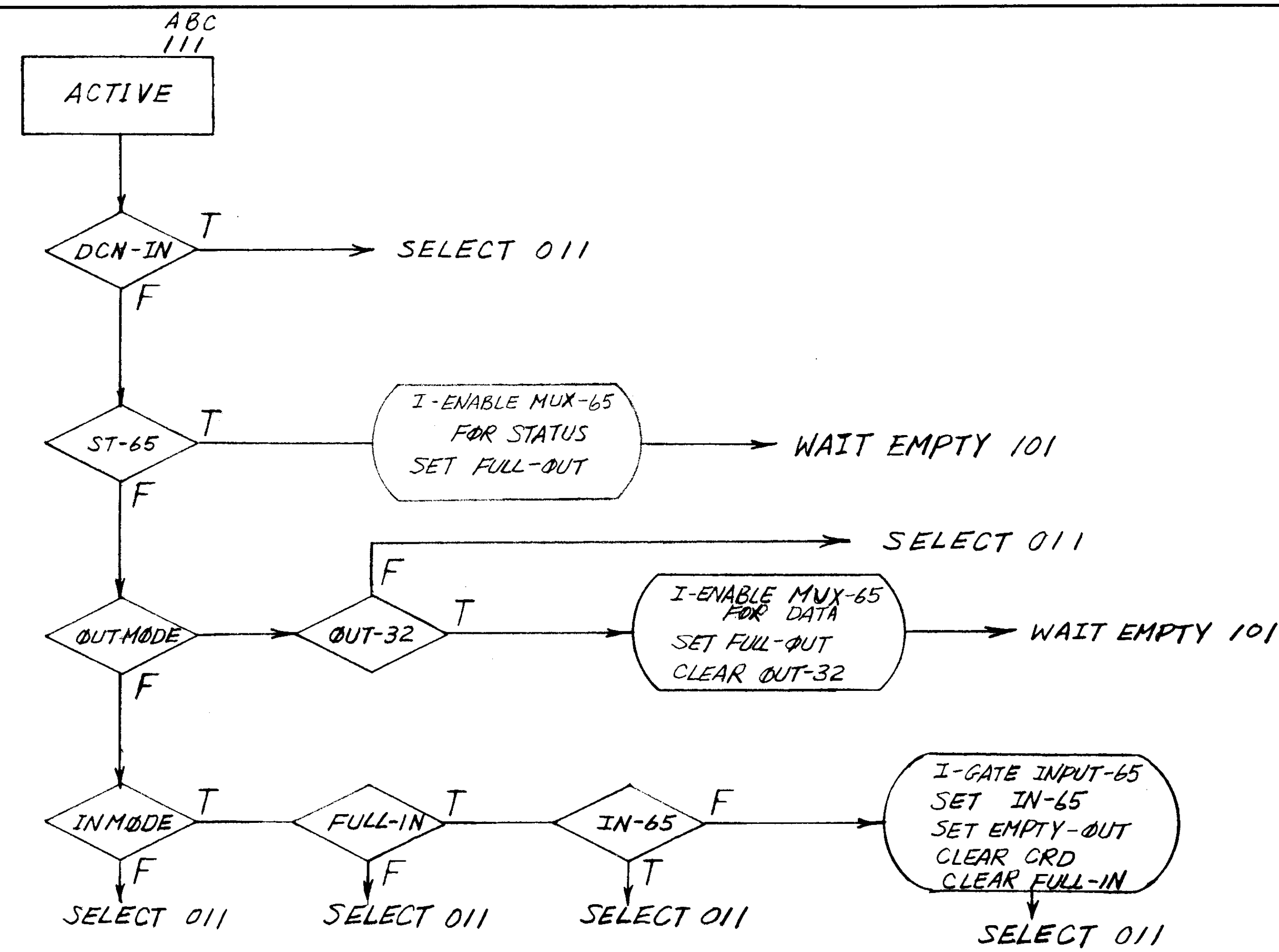


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— M65-2 SELECT

2

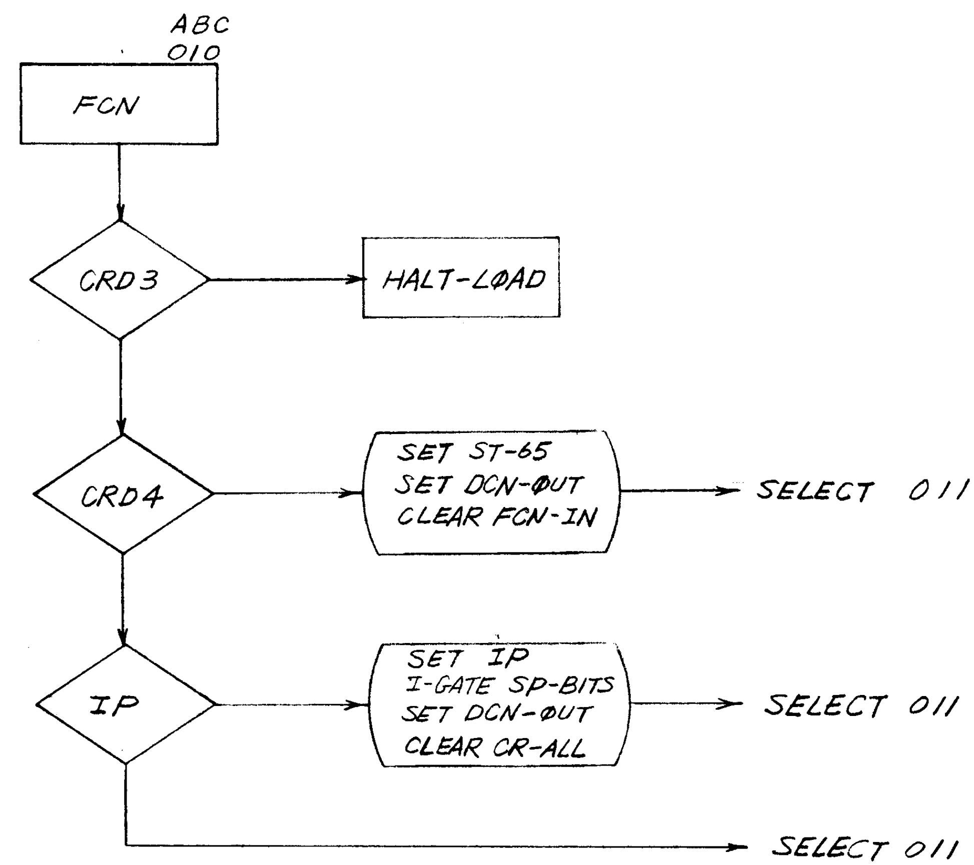


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— M65-3 ACTIVE

3

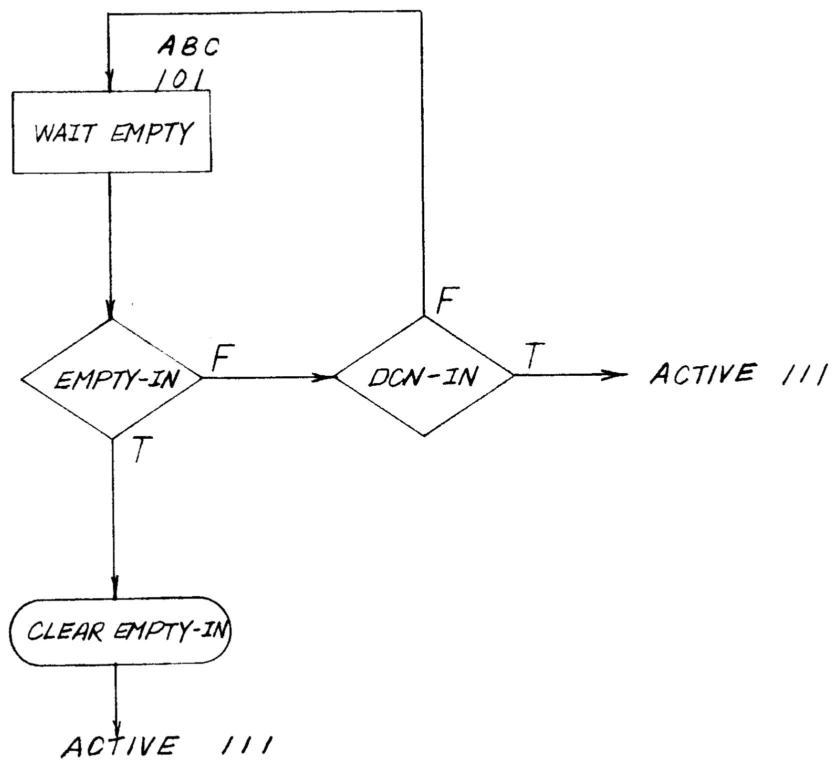


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— M65-4 FCN

4



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:_____ BY:_____ CHECKED:_____ APPROVED:_____ DATE:_____

TITLE— M65-5 WAIT EMPTY

5

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— M65-7

$Ka=B.C.(DCN\text{-}IN+\overline{ST\text{-}65}.\overline{OUT\text{-}MODE}+\overline{ST\text{-}65}.\overline{OUT\text{-}32})$

$Ja=B.C.(\overline{FCN\text{-}IN}.\overline{DCN\text{-}IN}.ACTIVE\text{-}IN)+B.\overline{C}.(CRD3)$

$Kb=\overline{A}.C.(FCN\text{-}IN.\overline{EQUIP})-A.C.(\overline{DCN\text{-}IN}.\overline{ST\text{-}65}+\overline{DCN\text{-}IN}.OUT\text{-}MODE.$

$OUT\text{-}32)+A.C$

$Jb=\overline{A}.C.(FCN\text{-}IN.EQUIP)+A.C.(EMPTY\text{-}IN+DCN\text{-}IN)$

$Kc=\overline{A}.\overline{B}.(\overline{FCN\text{-}IN}+\overline{EQUIP})+\overline{A}.B.(FCN\text{-}IN.EQUIP.\overline{DCN\text{-}IN})$

$Jc=\overline{A}.\overline{B}.(FCN\text{-}IN+EMPTY\text{-}IN)+\overline{A}.B.(\overline{CRD3})$

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ____ BY: ______ CHECKED: ______ APPROVED: ______ DATE: ______

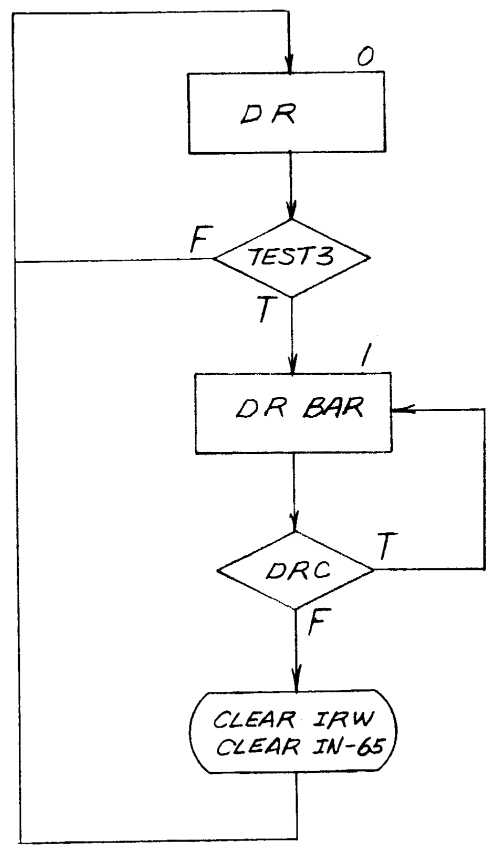
TITLE—

7

	OUT-32 OUT-MODE		ST-65	
OUTPUT-65	MODE OUTPUT-32	MODE OUTPUT-32	CRD11	CRD11
0	4 *	2 *	IP	
1	5	3	PF	PF
2	6	4	IN-MODE	ST-32
3	7	5	OUT-MODE	[illegible]RW
4	8	6	SP0	DCN-65
5	9	7	SP1	RT
6	10	10	SP2	ACK2
7	11	11	SP3	ACK
8	12	12	SP4	OUT-32
9	13	13	SP5	IN-65
10	14	14	SP6	MODE2
11	15	15	SP7	MODE

* = 0 IF HW - 1

7



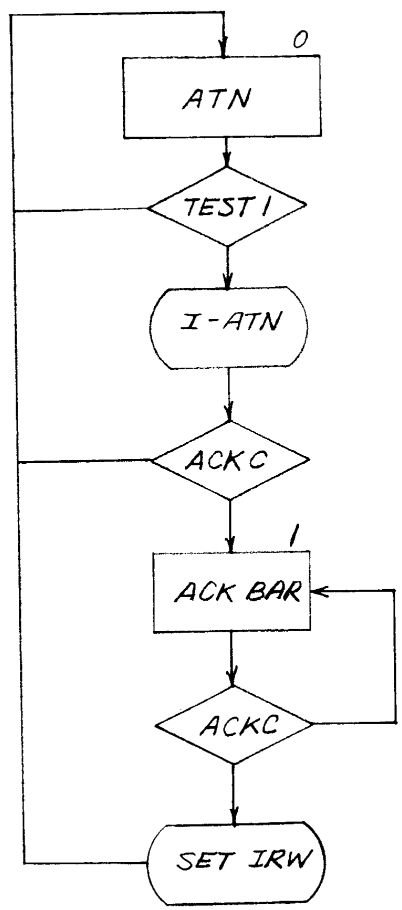
TEST 2 = IN-MØDE · IN-65 · ST-32
TEST 3 = TEST2 · DRC

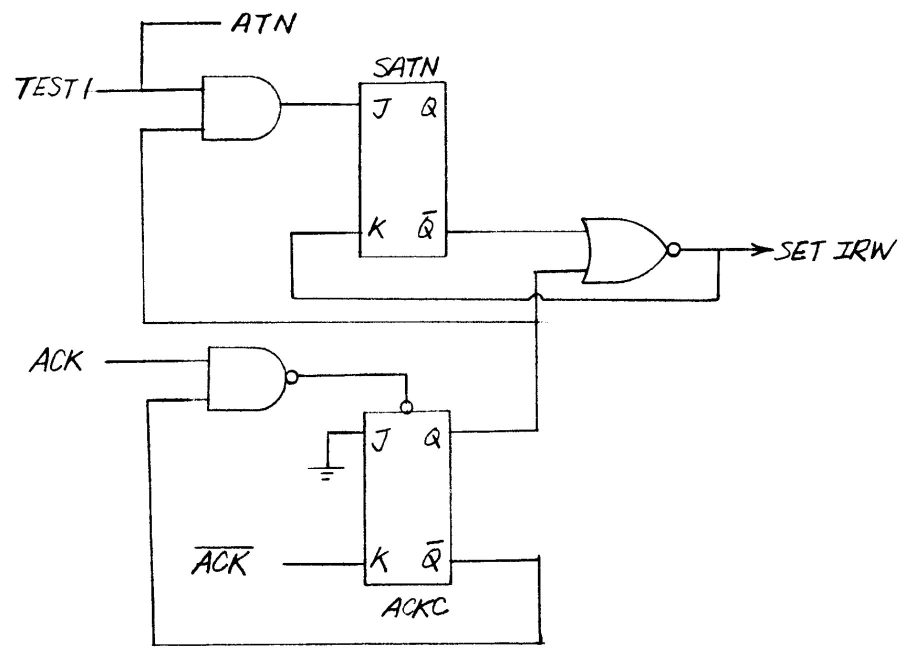
MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— M32-1 DR

8





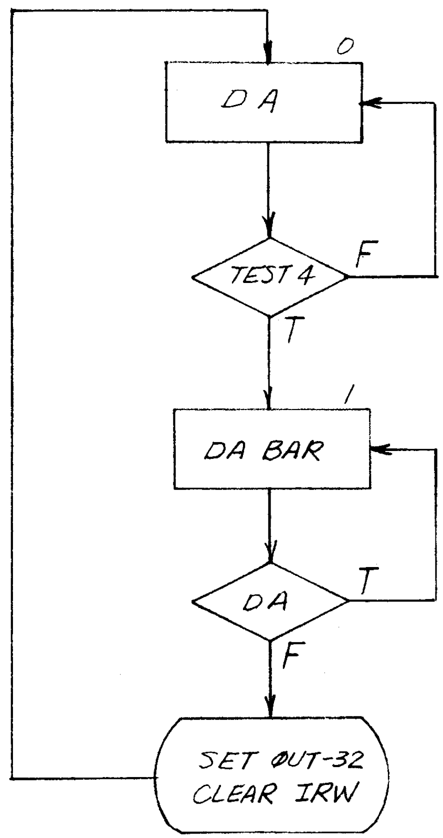
TEST 1 = IRW · RT · (IN-MODE · (IN-65 + DCN-65)
+ OUT-MODE · (OUT-32 + DCN-65))

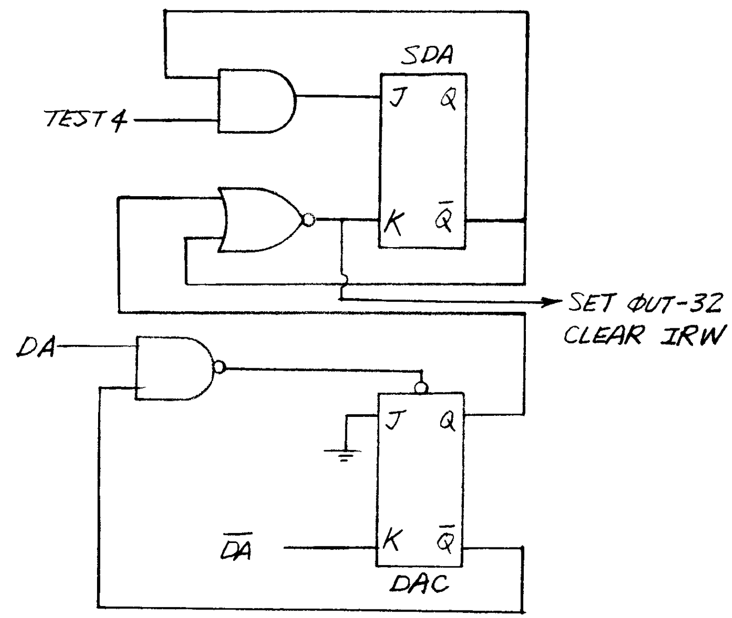
MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— M32-2 ATN

9





TEST 4 = ($\overline{ØUT\text{-}32}$ · ØUT-MØDE) · DAC

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ______ BY: ______ CHECKED: ______ APPROVED: ______ DATE: ______

TITLE— M32-3 DA

10

1. OUTOUTS FROM BACKPLACE

SR	-	STATUS REQUEST
DR	-	DATA REQUEST
CMD	-	COMMAND
DA	-	DATA AVAILABLE
ADRS	-	ADDRESS
RACK	-	ACKNOWLEDGE
CL07	-	POWER FAIL
SCLRO	-	POWER UP

2. INPUTS TO THE BACKPLACE

ATN	-	ATTENTION
SYN	-	SYNC
HW	-	HALFWORD MODE

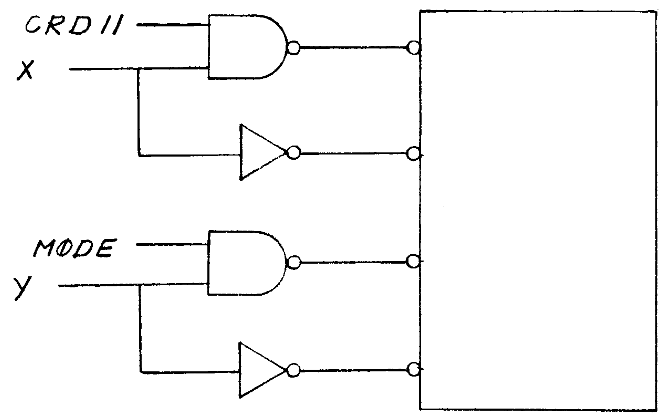
	$\overline{SR1}$	DR ST-32	DR TEST MODE	DR TEST2	$\overline{ACK}$	$\overline{ACK2}$	$\overline{DR2}$	
D00	0		0	0	0	0	0	IF HW-0 ALL 0 (D00–D06)
D01	0		0	0	0	0	0	
D02	0		CRD0	0				
D03	0		CRD1	0				
D04	0		CRD2	CRD0				
D05	0		CRD3	CRD1				
D06	0		CRD4	CRD2				
D07	0		CRD5	CRD3	0	0	0	
D08	IS0		0	CRD4	DA0	DA0	IP	
D09	IS1		0	CRD5	DA1	DA1	SP1	
D10	IS2		CRD6	CRD6	DA2	DA2	SP2	
D11	IS3		CRD7	CRD7	DA3	DA3	SP3	
D12	BSY		CRD8	CRD8	DA4	DA4	SP4	
D13	EX		CRD9	CRD9	DA5	DA5	SP5	
D14	EOM		CRD10	CRD10	DA6	DA6	SP6	
D15	BU	ST15	CRD11	CRD11	0	1	SP7	

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ______ BY: ______ CHECKED: ______ APPROVED: ______ DATE: ______

TITLE—

12



X = I-ENABLE MUX-65 FØR STATUS
Y = I-ENABLE MUX-65 FØR DATA

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— MUX-65

13

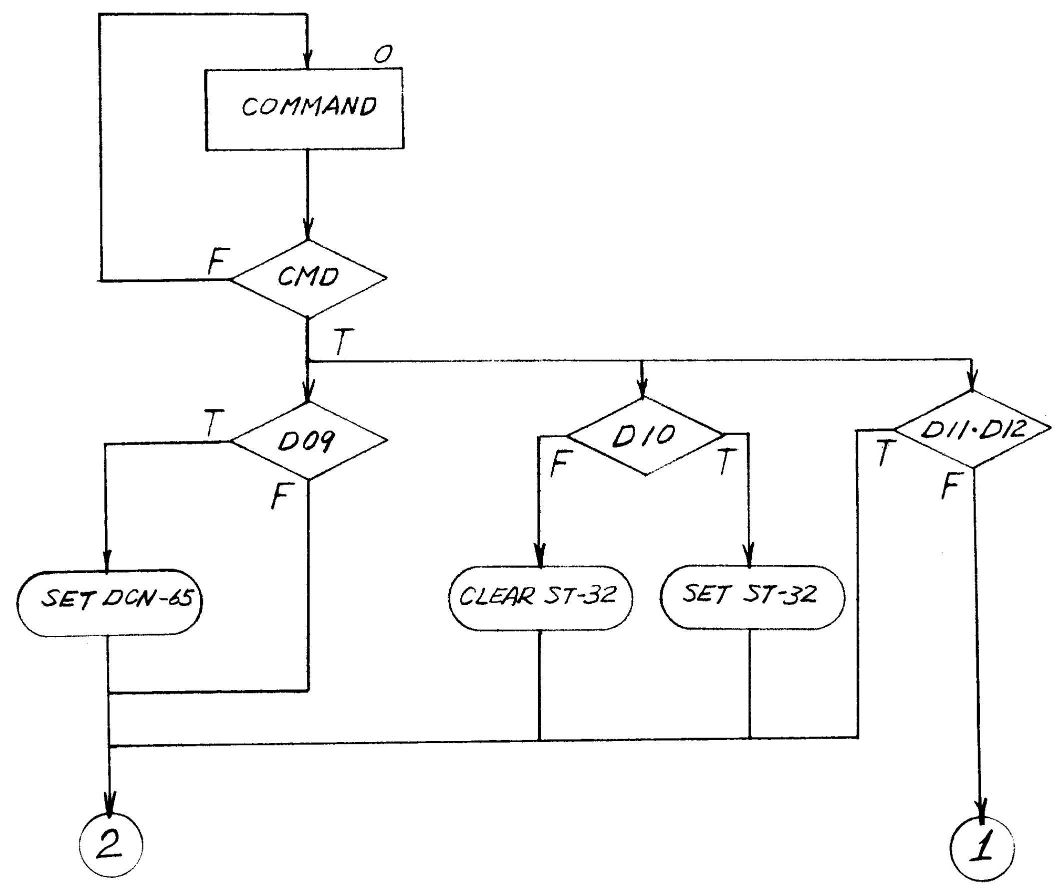
SR STATUS BITS

BIT	
0	$\overline{\text{ACN-IN}}$
1	$\overline{\text{IN-65}}$
2	$\overline{\text{OUT-32}}$
3	IP
4	$\overline{\text{IN-MODE.IN-65+OUT-MODE.}\overline{\text{OUT-32}}}$
5	RT
6	—
7	DCN-65.(IN-MODE.$\overline{\text{IN-65}}$+OUT-MODE)

COMMAND BITS

BIT	FUNCTION
D08	—
D09	SET DCN-OUT
D10	STATUS
D11	IN-MODE } BOTH=1, IGNORE REMAINDER OF COMMAND.
D12	OUT-MODE } BOTH=1, IGNORE REMAINDER OF COMMAND.
D13	RT
D14	MODE2
D15	MODE

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY
FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____
TITLE— COMMAND-2

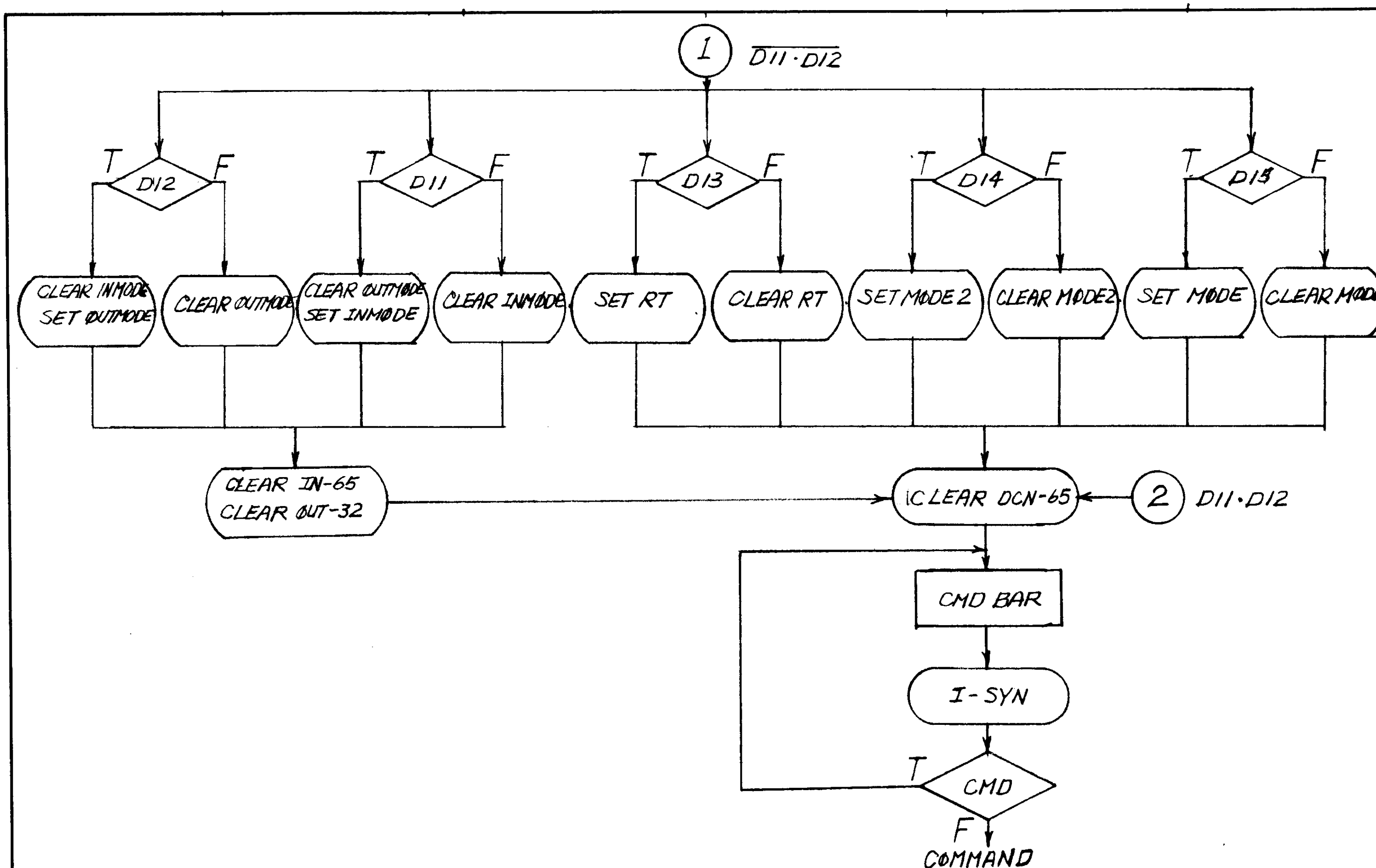


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ______ BY: ______ CHECKED: ______ APPROVED: ______ DATE: ______

TITLE— COMMAND -3

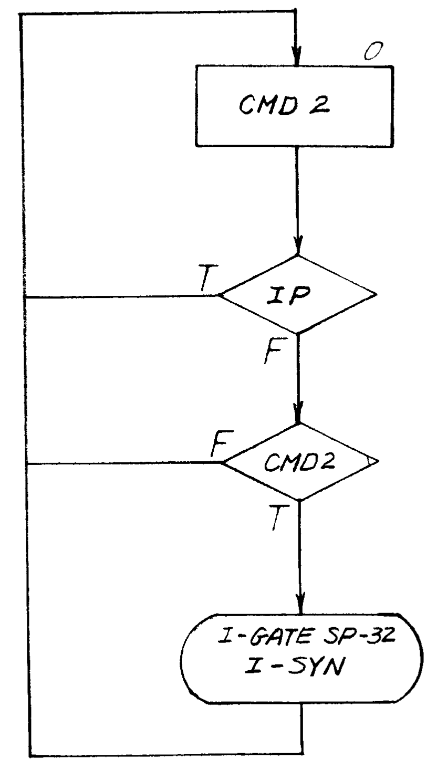
16



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— COMMAND-4

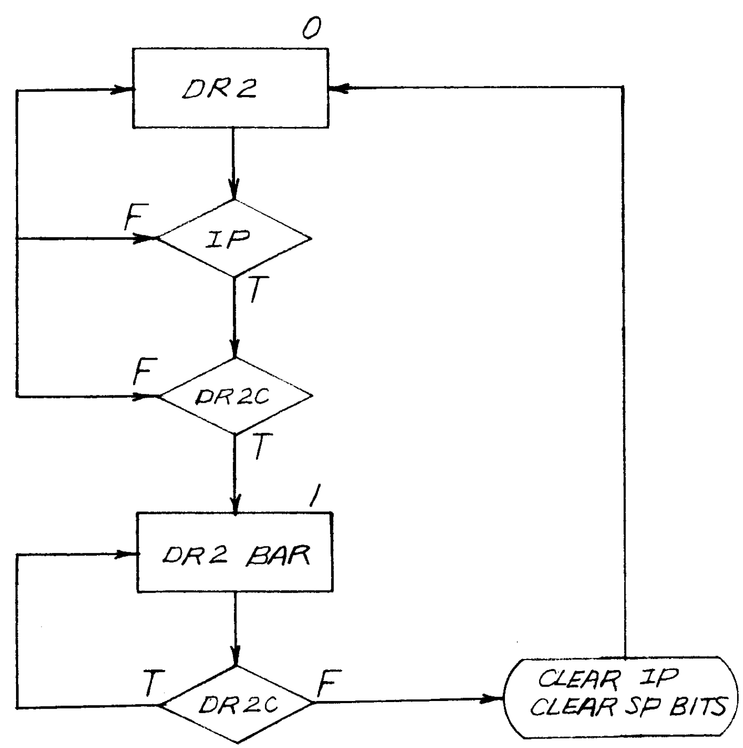


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:_____ BY:_____ CHECKED:_____ APPROVED:_____ DATE:_____

TITLE— CMD2

18



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— MINT-1

19

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE—

20

OUT-MUX 20

1. DCN-65 (6500SETDCN) Y

2. SET BY: $\overline{A}$(65).B(65).C(65).($\overline{\text{FCN-IN}}$.DCN-IN.$\overline{\text{ST-65.}}$(IN-MODE+OUT-MODE)

   CLEARED:BY: COMMAND

2. ST-65 N

   SET BY: $\overline{A}$(65).B(65).$\overline{C}$(65).($\overline{\text{CRD3}}$.$\overline{\text{CRD4}}$)

   CLEARED BY: $\overline{A}$(65).B(65).C(65).($\overline{\text{FCN-IN}}$.DCN-IN.ST-65)

3. IP Y

   SET BY: $\overline{A}$(65).B(65).$\overline{C}$(65).($\overline{\text{CRD3}}$.CRD4)

   CLEARED BY: DR2.BAR.($\overline{\text{DR2C}}$)

4. EMPTY-OUT N

   SET BY: A(65).B(65).C(65).($\overline{\text{DCN-IN}}$.ST-65.IN-MODE.FULL-IN.$\overline{\text{IN-65}}$)

   CLEARED BY:

5. EMPTY-OUT N

   SET BY: A(65).B(65).C(65).($\overline{\text{DCN-IN}}$.ST-65+OUT-MODE.OUT-32)

   CLEARED BY:

6. IN-65 YY

   SET BY: A(65)B(65)C(65).($\overline{\text{DCN-IN}}$.$\overline{\text{ST-65}}$.IN-MODE.FULL-IN)

   CLEARED BY: DR BAR.($\overline{\text{DRC}}$)

7. OUT-32 Y

   SET BY: DA BAR.($\overline{\text{DAC}}$)

   CLEARED BY: A(65)B(65)CC(65),($\overline{\text{DCN-IN}}$.$\overline{\text{ST-65}}$.OUT-MODE)

8. DCN-OUT N

   SET BY: $\overline{A}$(65).B(65).$\overline{C}$(65).($\overline{\text{CRD3}}$.($\overline{\text{CRD4}}$-IP))+COMMAND(D09)

   CLEARED BY:

9. IRW Y

   SET BY: ACK BAR.($\overline{\text{ACKC}}$)

   CLEARED BY: DA BAR.($\overline{\text{DAC}}$)+DR BAR.($\overline{\text{DRC}}$)

OUT-MUX 21

10. MODE Y

SET BY: COMMAND.(D15.($\overline{D11.D12}$))

CLEARED BY: COMMAND.($\overline{D15}$.($\overline{D11.D12}$))

11. MODE2 Y

SET BY: COMMAND.(D14.($\overline{D11.D12}$))

CLEARED BY: COMMAND.($\overline{D14}$.($\overline{D11.D12}$))

12. RT Y

SET BY: COMMAND.(D13.($\overline{D11.D12}$))

CLEARED BY: COMMAND.($\overline{D13}$.($\overline{D11.D12}$))

13. OUT-MODE Y

SET BY: COMMAND.(D12.$\overline{D11}$)

CLEARED BY: COMMAND.($\overline{D12}$)

14. IN-MODE Y

SET BY: COMMAND.(D11.$\overline{D12}$)

CLEARED BY: COMMAND.($\overline{D11}$)

15. ST-32 Y

SET BY: COMMAND.(D10)

CLEARED BY: COMMAND.($\overline{D10}$)

16. PF Y

SET BY: CLR07

CLEARED BY: CLEAR

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE—

ACTIVE ≡ S(111)-≡ $\overline{ABC}$

Ka ≡ $\text{ABC}.\text{DCN-IN}+\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.(\overline{\text{OUT-MODE}}+\overline{\text{OUT-32}})$

KA ≡ $\text{ABC}.\overline{\text{DCN-IN}}.\text{ST-65}+\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.\text{OUT-MODE}.\text{OUT-32}$

MUX 65-ST≡ $\text{ABC}.\overline{\text{DCN-IN}}.\text{ST-65}$

FULL-OUT≡$\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}+\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.\text{OUT-MODE}.\text{OUT-32}$

INPUT-65-≡ $\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.\text{IN-MODE}.\text{FULL-IN}.\overline{\text{IN-65}}$

IN-65 ≡ $\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.\text{IN-MODE}.\text{FULL-IN}.\overline{\text{IN-65}}$

EMPTY-OUT ≡ $\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.\text{IN-MODE}.\text{FULL-IN}.\overline{\text{IN-65}}$

CLEARED CRD ≡ $\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.\text{IN-MODE}.\text{FULL-IN}.\overline{\text{IN-65}}$

CLEARED FULLIN≡$\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.\text{IN-MODE}.\text{FULL-IN}.\overline{\text{IN-65}}$

CLEARED OUT-32 ≡ $\text{ABC}.\overline{\text{DCN-IN}}.\overline{\text{ST-65}}.\text{OUT-MODE}.\text{OUT-32}$

FCN ≡ S(010) ≡ $\overline{\bar{A}B\bar{C}}$

Ja ≡ $\bar{A}B\bar{C}.\text{CRD3}$

ST-65 ≡ $\bar{A}B\bar{C}.\overline{\text{CRD3}}.\overline{\text{CRD4}}$

DCN-OUT ≡ $\bar{A}B\bar{C}.\overline{\text{CRD3}}.\overline{\text{CRD4}}+\bar{A}B\bar{C}.\overline{\text{CRD3}}.\text{CRD4}.\overline{\text{IP}}$

CLEARED DCN-IN ≡ $\bar{A}B\bar{C}.\overline{\text{CRD3}}.\overline{\text{CRD4}}$

Jc ≡ $\bar{A}B\bar{C}.\overline{\text{CRD3}}$

IP-≡$\bar{A}B\bar{C}.\overline{\text{CRD3}}.\text{CRD4}.\overline{\text{IP}}$

CLEAR CR-ALL ≡ $\bar{A}B\bar{C}.\overline{\text{CRD3}}.\text{CRD4}.\overline{\text{IP}}$

SP-BITS ≡ $\bar{A}B\bar{C}.\overline{\text{CRD3}}.\text{CRD4}.\overline{\text{IP}}$

WAIT EMPTY ≡ S(101) ≡ $\overline{A\bar{B}C}$

Jβ ≡ $(A\bar{B}C.\text{EMPTY-IN})+(A\bar{B}C.\text{DCN-IN})$

CLEAR EMPTY-IN-≡ $A\bar{B}C.\text{EMPTY-IN}$

22

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ___ BY: ___ CHECKED: ___ APPROVED: ___ DATE: ___

TITLE—

23

INITIAL = S(000) = $\overline{\bar{A}\bar{B}\bar{C}}$

Ja = $\bar{A}\bar{B}\bar{C}$(FCN-IN+FULL-IN+DCN-IN+ACTIVE+EMPTY) = INITIALS

INITIAL[illegible] = S(001) = $\overline{\bar{A}\bar{B}C}$

CLEAR CR-ALL = $\bar{A}\bar{B}C$.($\overline{\text{FCN-IN}}$+$\overline{\text{EQUIP}}$)

Jb = $\bar{A}\bar{B}C$.FCN-IN.EQUIP = INITIAL[illegible]T

Kc = $\bar{A}\bar{B}C$.($\overline{\text{FCN-IN}}$+$\overline{\text{EQUIP}}$) = INITIAL[illegible]S

SELECT = S(011) = $\overline{\bar{A}BC}$

CLEAR CR-ALL = $\bar{A}BC$.DCN-IN.(EQUIP.FCN-IN+$\overline{\text{FCN-IN}}$)

CLEAR ST-65 = $\bar{A}BC$.$\overline{\text{FCN-IN}}$.DCN-IN

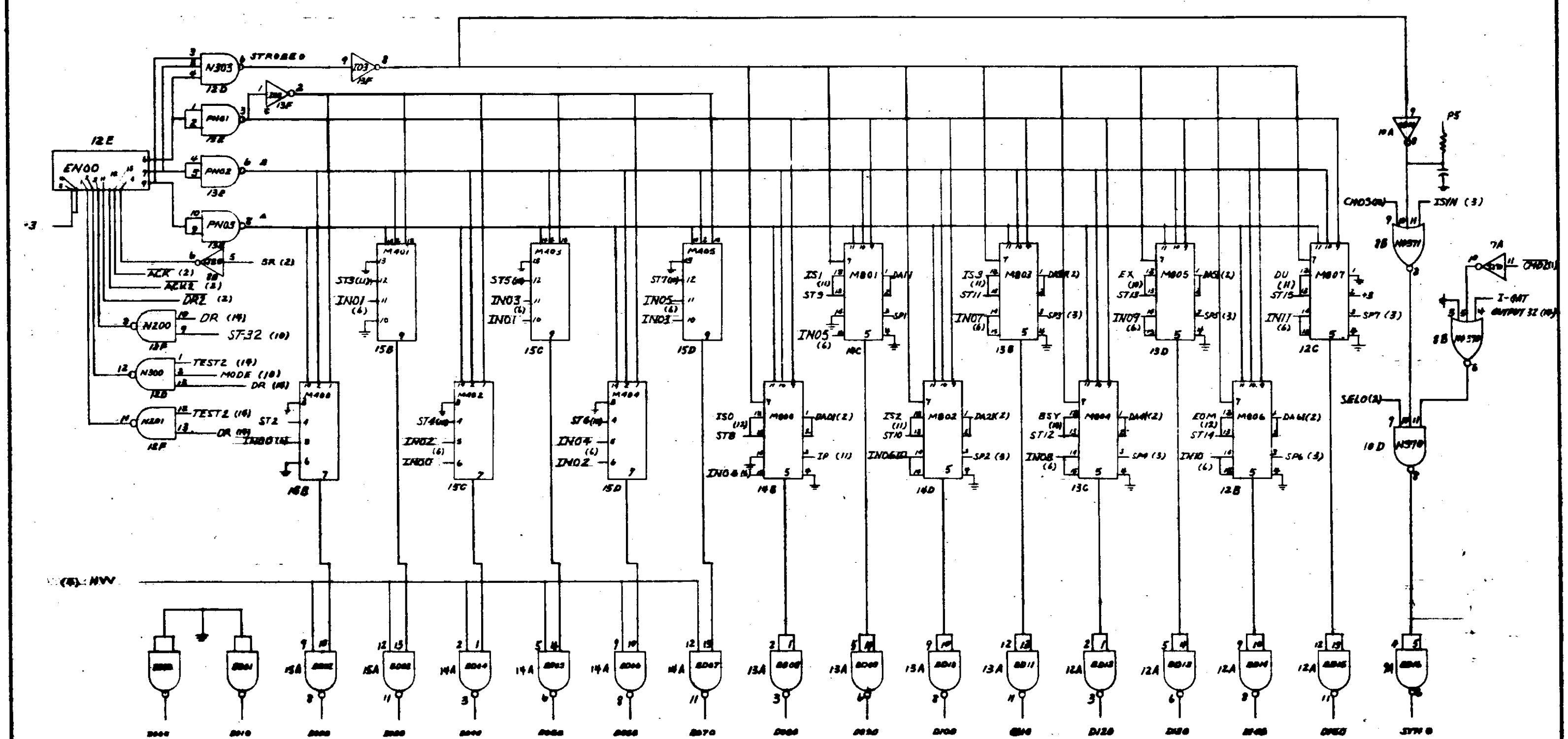
DCN-65 = $\bar{A}BC$.$\overline{\text{FCN-IN}}$.DCN-IN.~~AST+65~~(IN-MODE + OUT-MODE)

Ja = $\bar{A}BC$.$\overline{\text{FCN-IN}}$.$\overline{\text{DCN-IN}}$.ACTIVE-IN

Ka = $\bar{A}BC$.FCN-IN.$\overline{\text{EQUIP}}$

Kc = $\bar{A}BC$.FCN-IN.EQUIP.$\overline{\text{DCN-IN}}$ = SELECTU

BDXX - SN7438	A3XX - SN74S11	BNXX - SN74147	N3XX - SN74S10
PNXX - SN7437	IXX - SN74S04	IØXX - SN74S05	NØXX - SN7427
M4XX - SN74153	M8XX - SN74161A	N2XX - SN74S00	



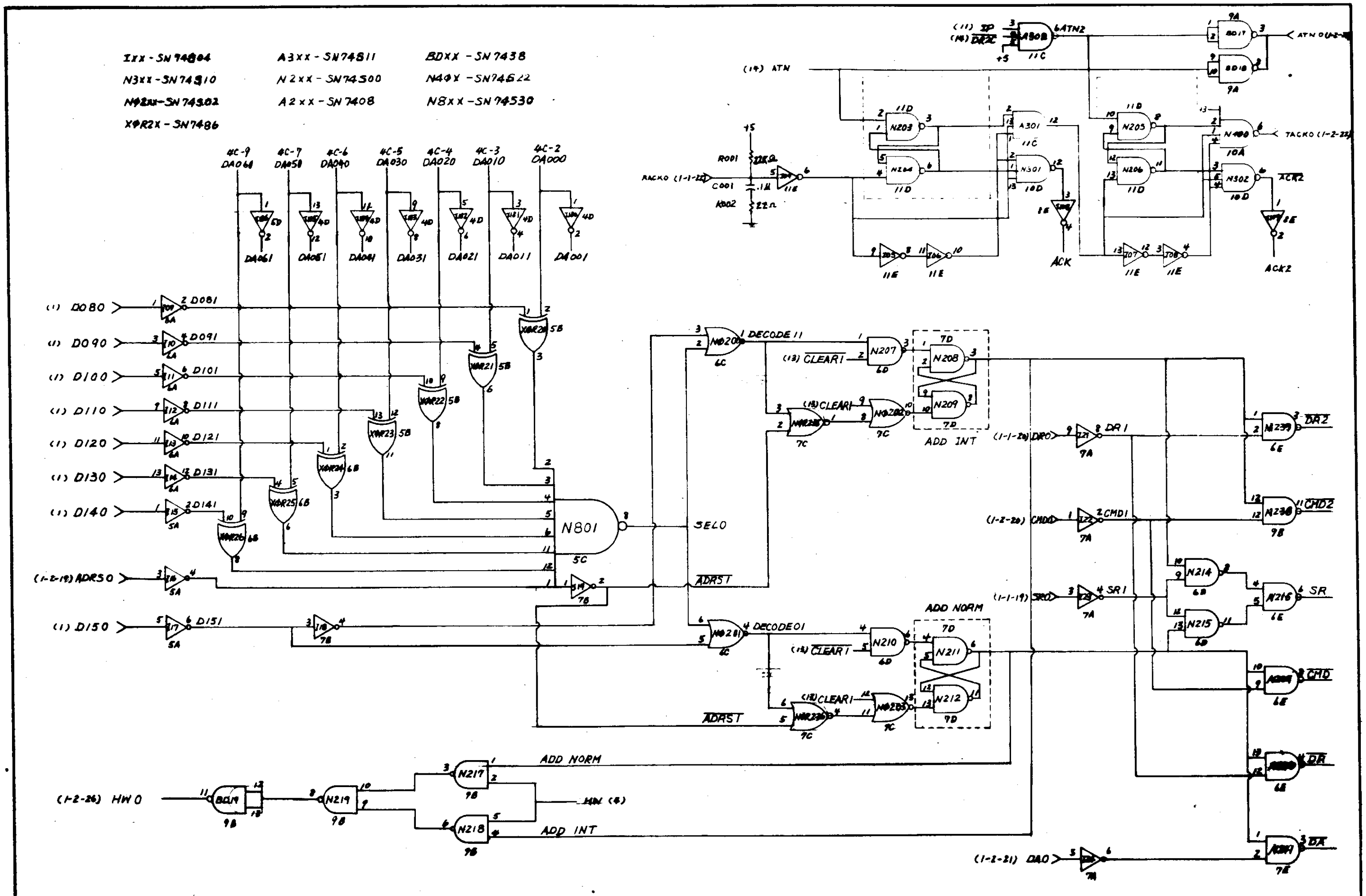
7/32 Front-End (A)

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ______ BY: PAG CHECKED: ______ APPROVED: ______ DATE: ______

TITLE— ESELCH BUS INPUT

1



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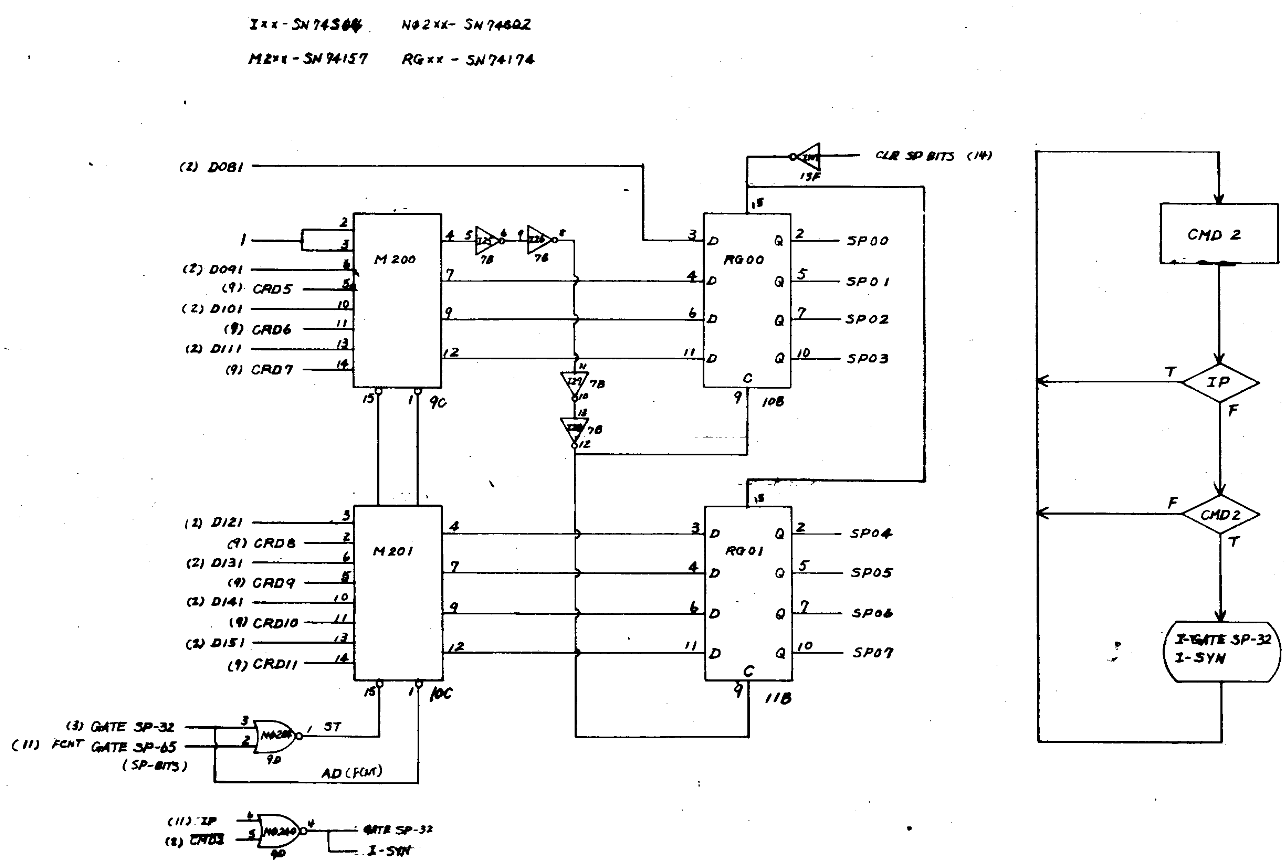
FOR: ____ BY: ____ CHECKED: ____ APPROVED: ____ DATE: ____

TITLE— ADRS. SELECTOR AND INT. CONTROL

2

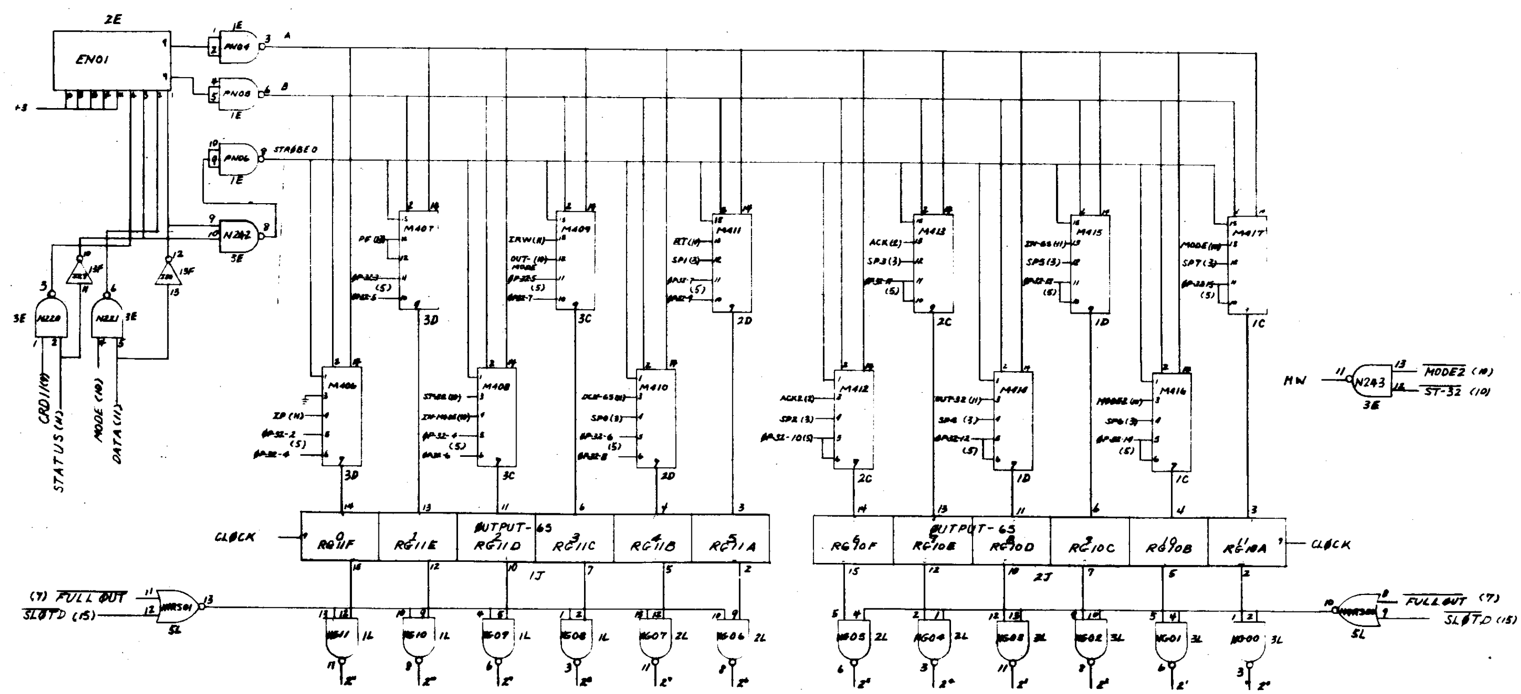


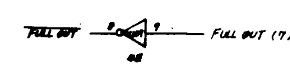
MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: BY: Peter CHECKED: APPROVED: DATE: May 30, 1974

TITLE— SP REGISTER AND CONTROL

3





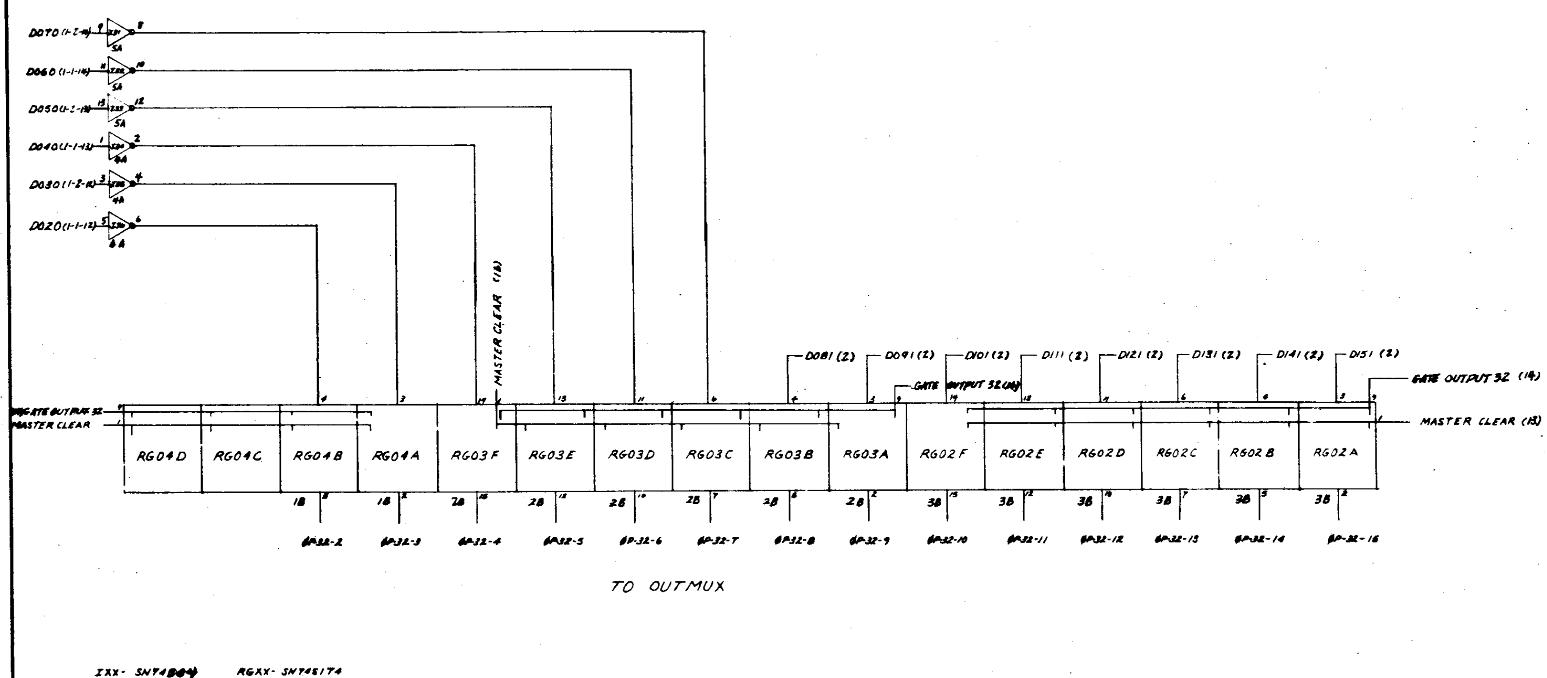
ENXX- SN74147 PNXX-SN7437 IXX SN74S04 N4XY- SN74S22
N2XX - SN74S00 M4XX - SN74153 N3XX - SN74S02 GXX- SN74S08
OUTPUT-65 - SN74S174

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:_____ BY:_____ CHECKED:_____ APPROVED:_____ DATE:_____

TITLE— OUTMUX / OUTPUT-65

4

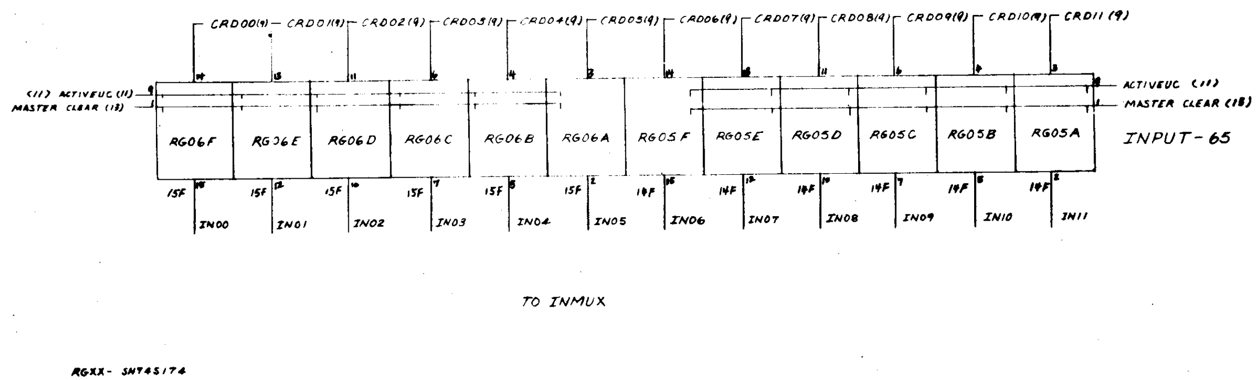


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ____ BY: GB CHECKED: ________ APPROVED: ________ DATE: ________

TITLE— OUTPUT-32

5

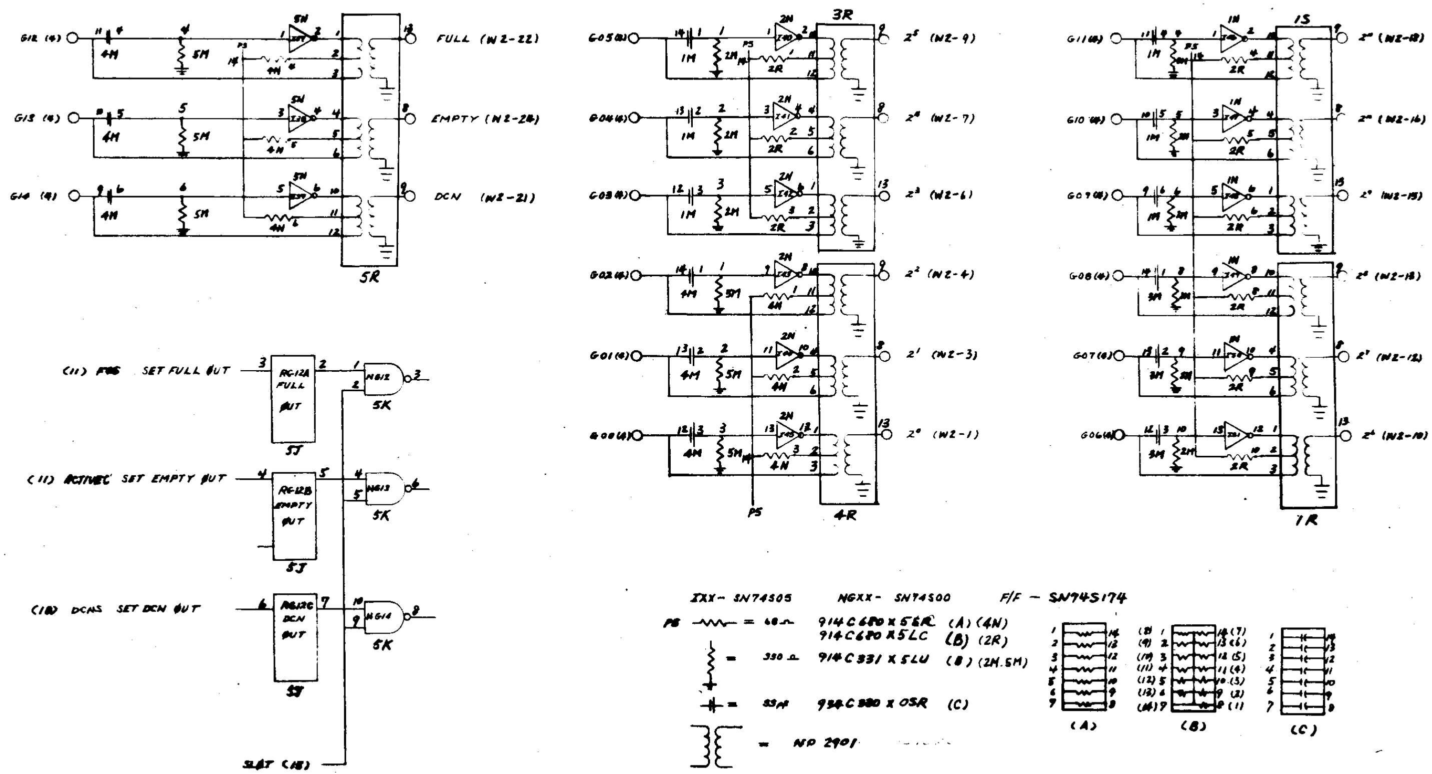


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE— INPUT-65

6

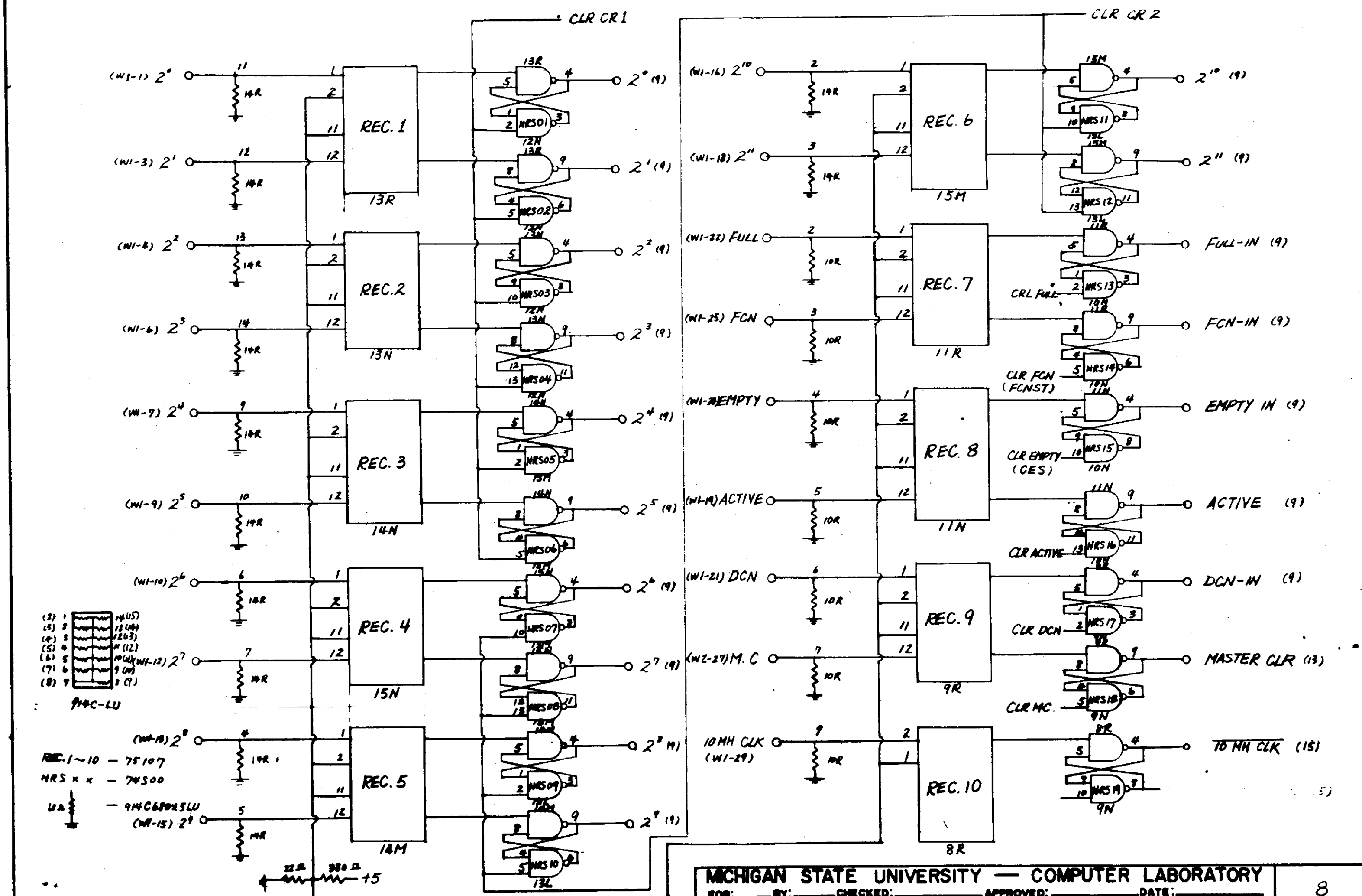


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ______ BY: RAB CHECKED: ______ APPROVED: ______ DATE: ______

TITLE— 6000 TRANSMITTERS

7

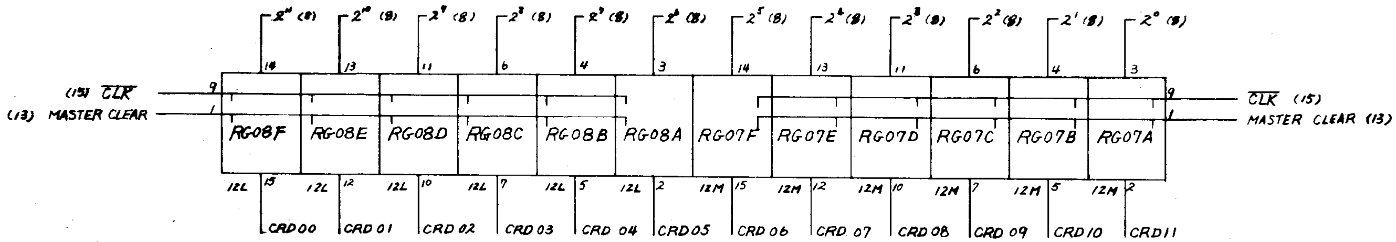


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

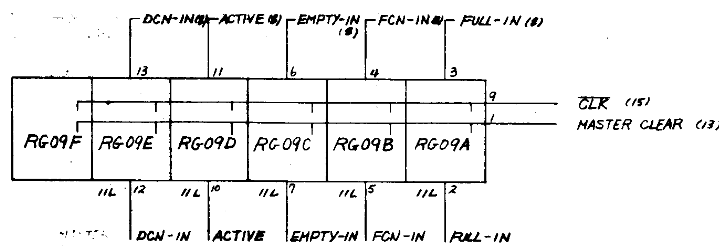
FOR: BY: CHECKED: APPROVED: DATE:

TITLE— RCVR & CRD-SR

8



INPUT – 65



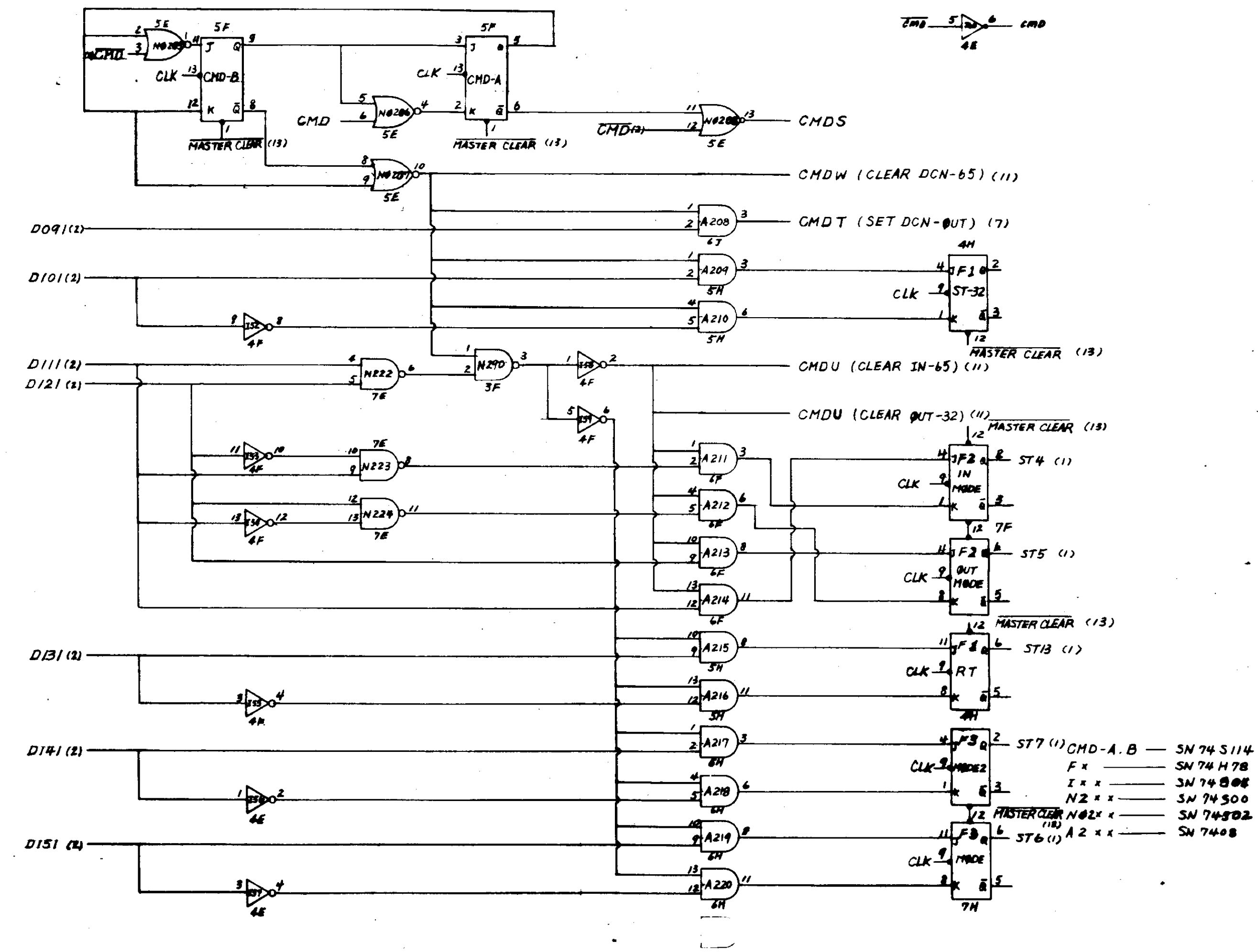
RGxx – SN74S174

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ____ BY: ____ CHECKED: ____ APPROVED: ____ DATE: ____

TITLE— CRD-D

9

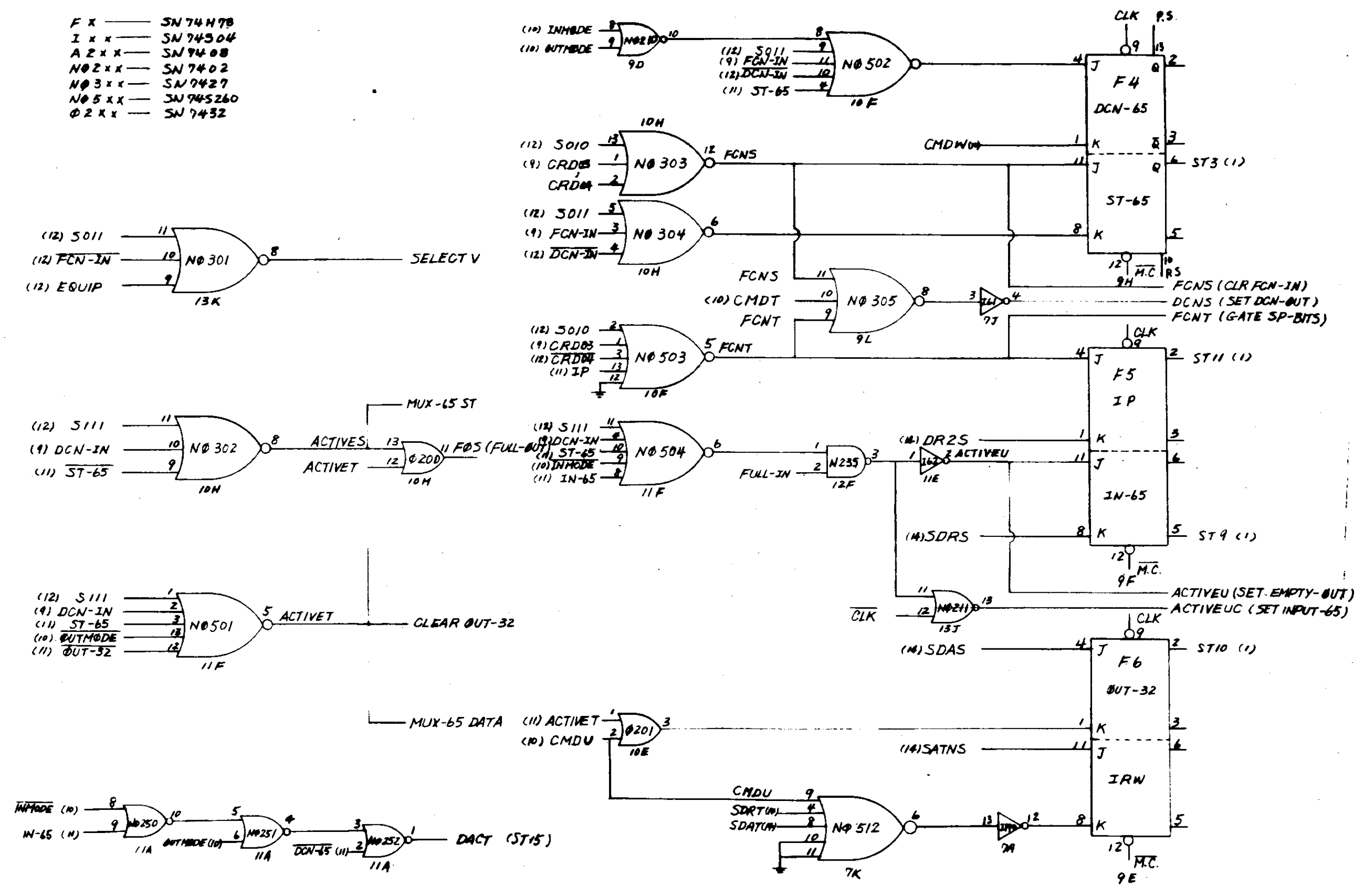


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ____ BY: ____ CHECKED: ____ APPROVED: ____ DATE: ____

TITLE— COMMAND

10

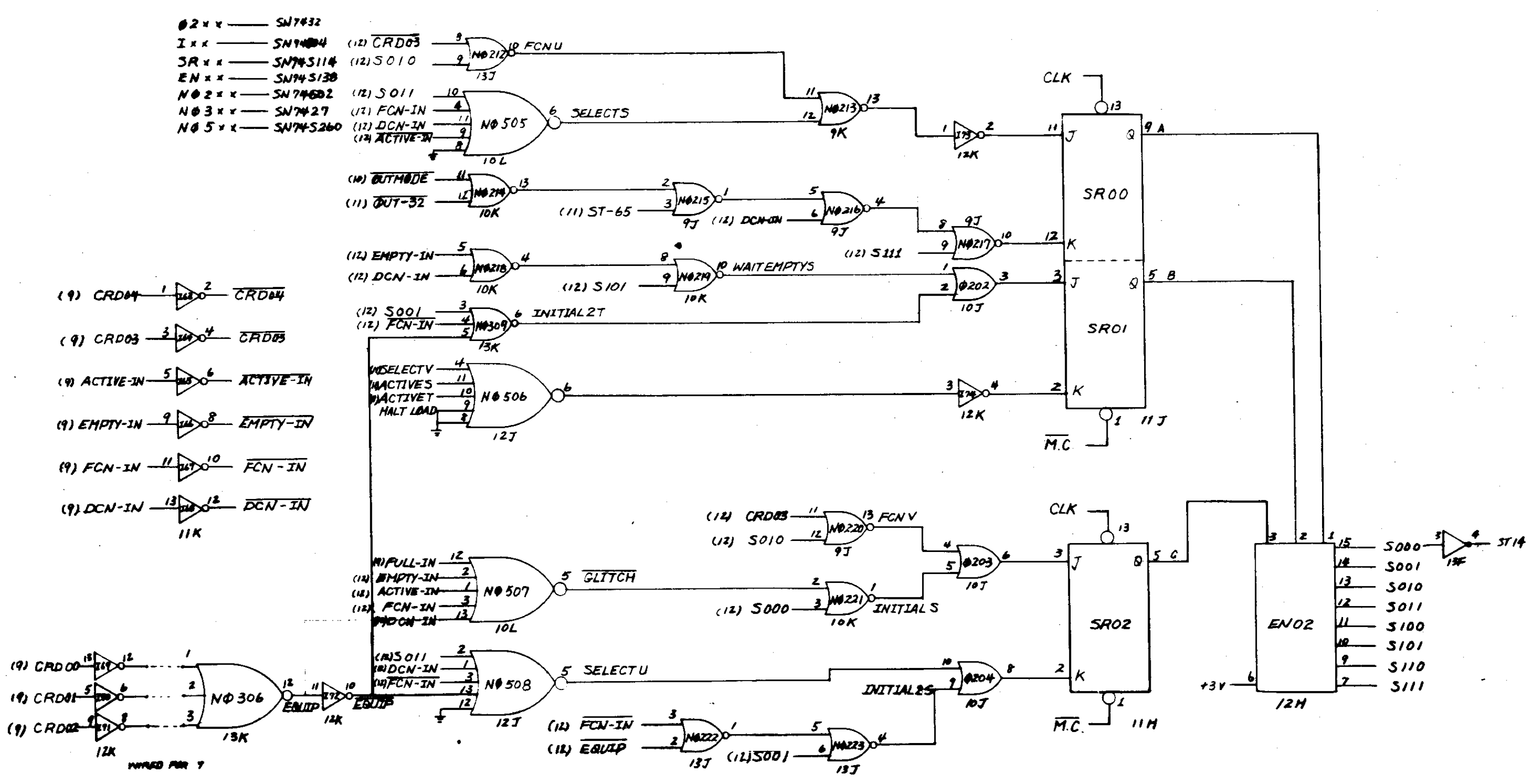


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ______ BY: ______ CHECKED: ______ APPROVED: ______ DATE: ______

TITLE—DCN-65, ST-65, IP, IN-65, OUT-32, IRW

11

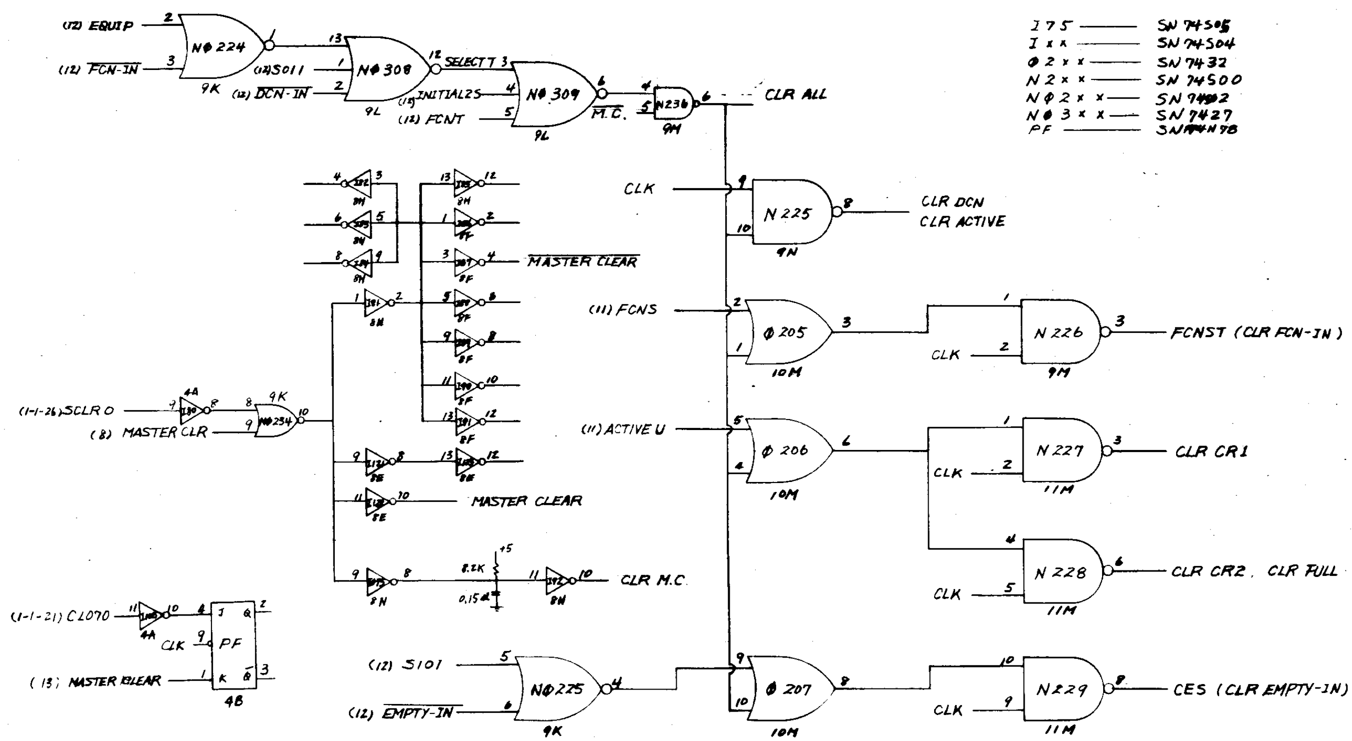


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: BY: CHECKED: APPROVED: DATE:

TITLE— M-65

12

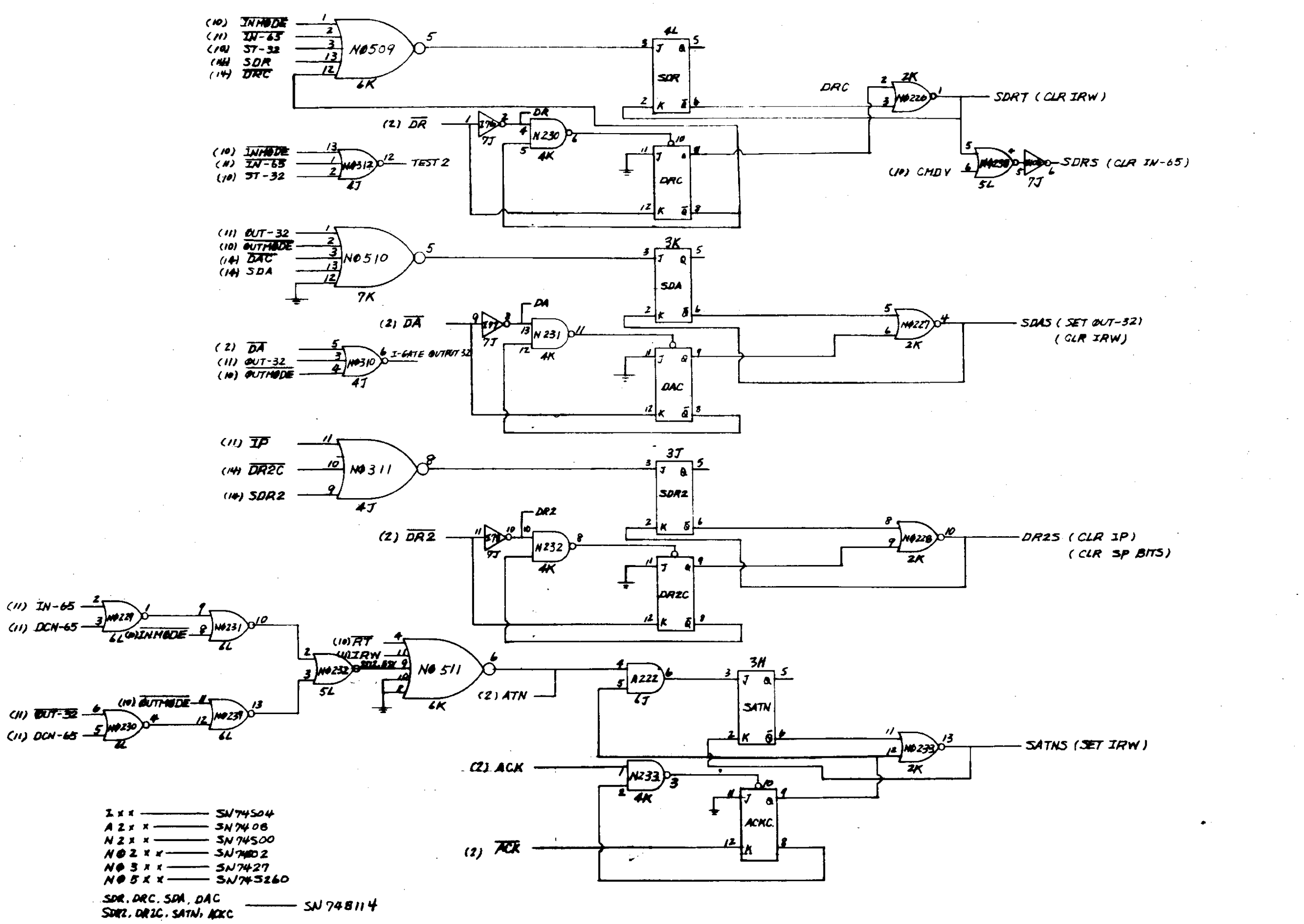


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: BY: CHECKED: APPROVED: DATE:

TITLE— CLR CRC, CRD, PF

13

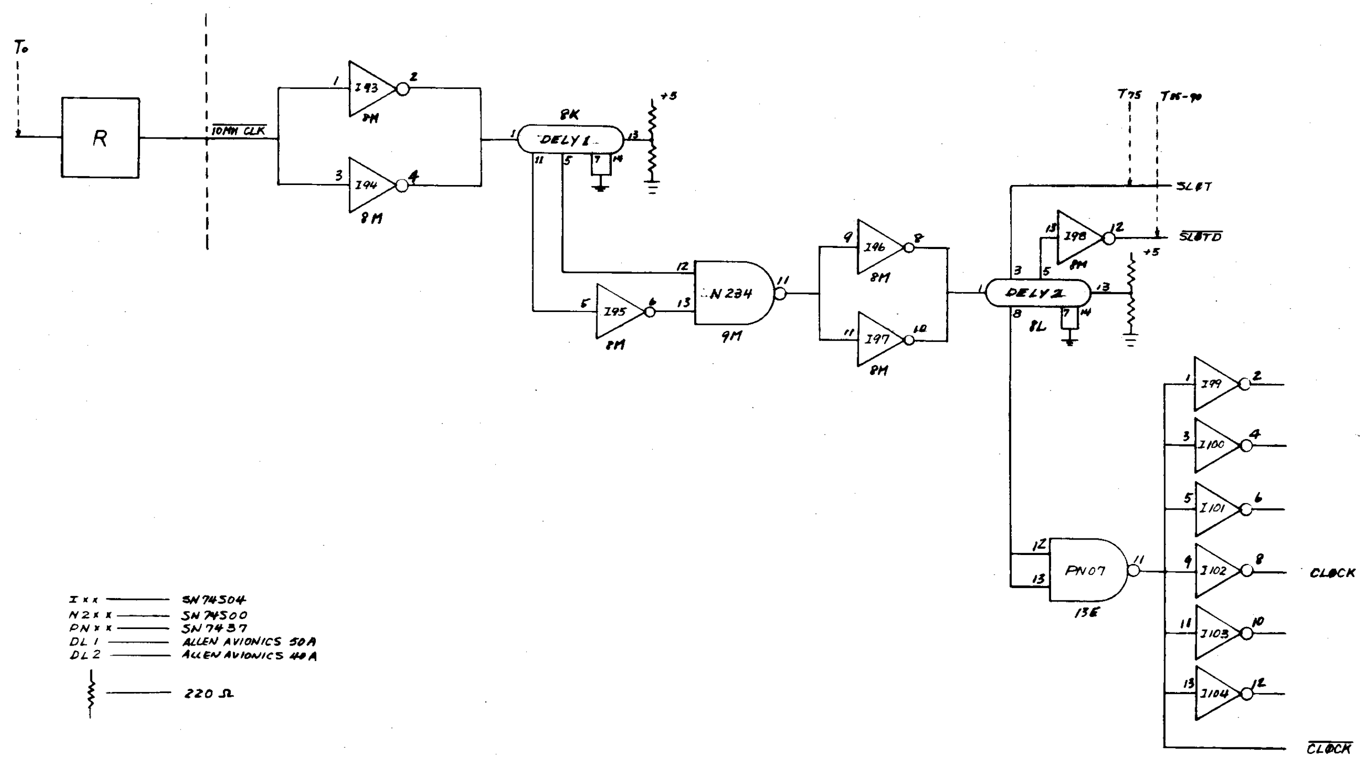


MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: BY: CHECKED: APPROVED: DATE:

TITLE— DR, DA, MINT-1, ATN

14



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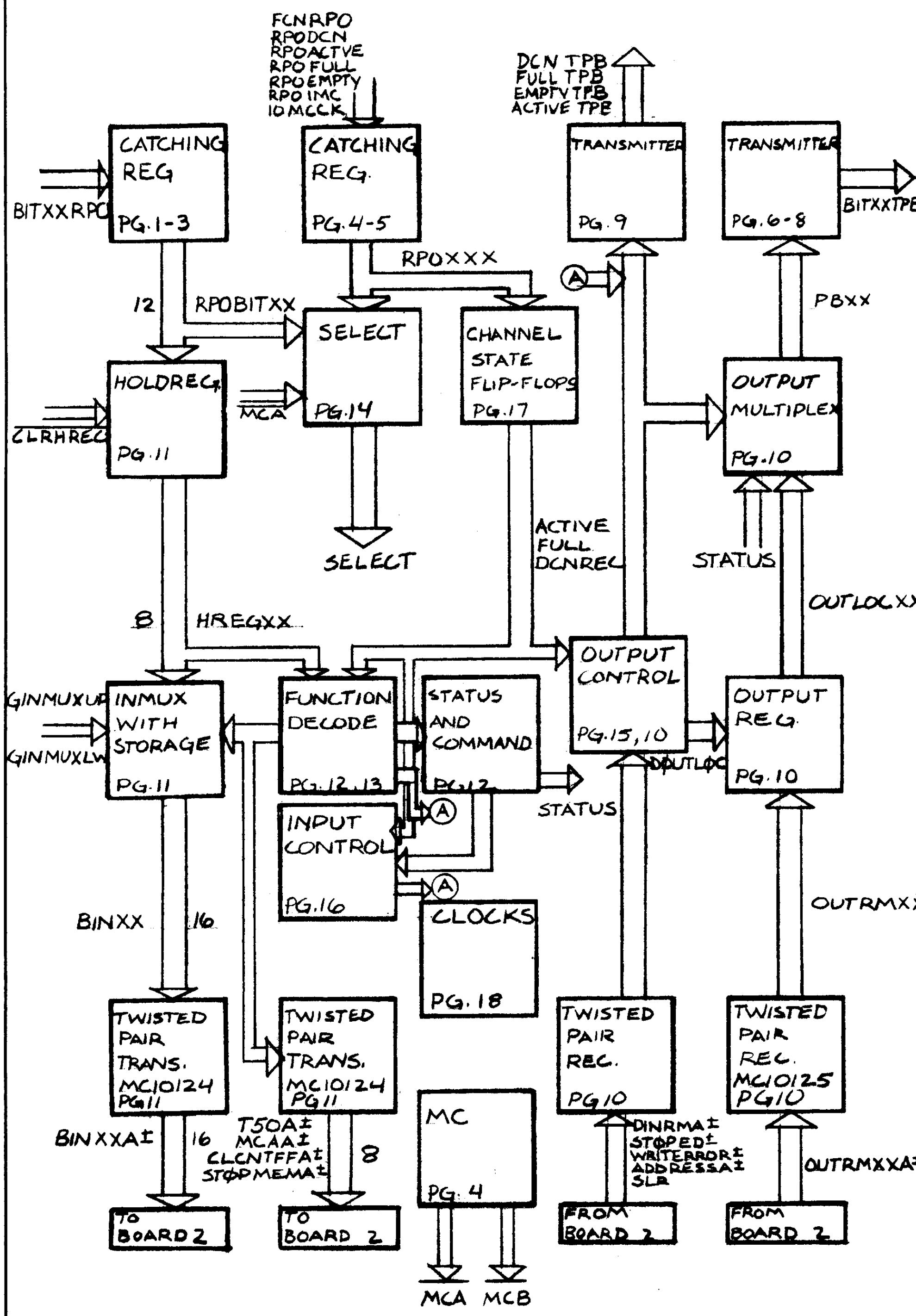
FOR:_____ BY:_____ CHECKED:_____ APPROVED:_____ DATE:_____

TITLE— SLØT MECHINE

15



7/32 Front-End (B) ?

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ____ BY: ____ CHECKED: ____ APPROVED: ____ DATE: ____

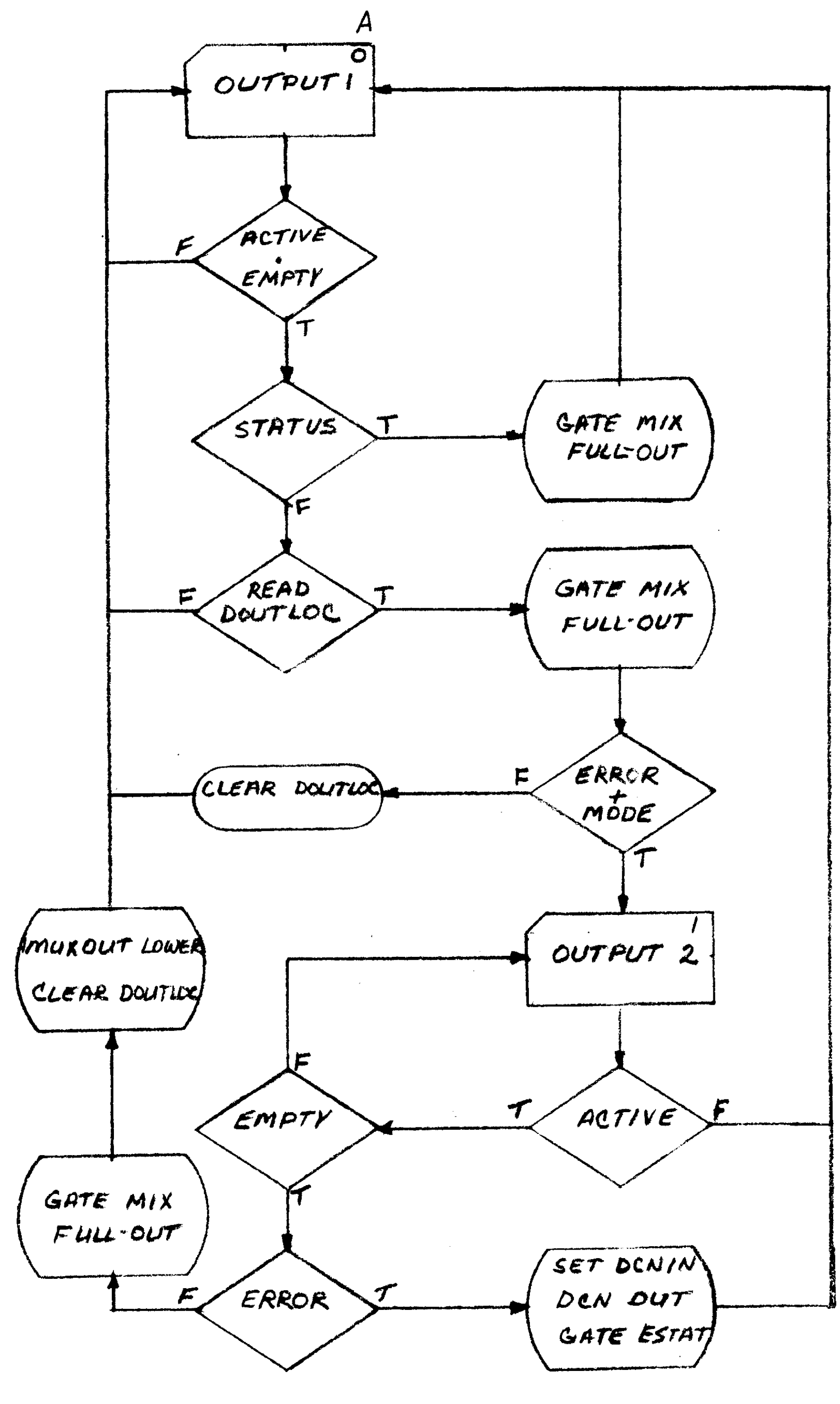
TITLE—

OUTPUT H	=	$(\mathrm{OUTPUT\ A} \downarrow \mathrm{STATUS}) \downarrow \mathrm{OUTPUT}$
OUTPUT A	=	$\overline{\mathrm{READ}} \downarrow \overline{\mathrm{DOUTLOC}}$
OUTPUT B	=	$\overline{\mathrm{ACTIVE}} \downarrow \overline{\mathrm{EMPTY}}$
OUTPUT C	=	$\mathrm{ERROR} \downarrow \mathrm{MODE}$
OUTPUT D	=	$\mathrm{OUTPUT\ A} \uparrow \mathrm{OUTPUT\ B}$
JOUTPUT	=	$\mathrm{ACTIVE} \cdot \mathrm{EMPTY}\ \mathrm{READ} \cdot \mathrm{DOUTLOC}$
		$\cdot (\mathrm{ERROR} + \mathrm{MODE})$
	=	$\mathrm{OUTPUT\ D} \downarrow \mathrm{OUTPUT\ C}$
OUTPUT E	=	$\mathrm{OUTPUT\ D} \downarrow \mathrm{OUTPUT}$
OUTPUT F	=	$\overline{\mathrm{OUTPUT}} \downarrow \mathrm{ERROR}$
OUTPUT G	=	$\mathrm{OUTPUT\ B} \downarrow \mathrm{OUTPUT\ F}$
KDOUTLOC	=	$\mathrm{ACTIVE} \cdot \mathrm{EMPTY} \cdot \mathrm{READ} \cdot \mathrm{DOUTLOC}$
		$\cdot \overline{\mathrm{OUTPUT}} \cdot (\overline{\mathrm{ERROR} + \mathrm{MODE}})$
		$+ \mathrm{OUTPUT} \cdot \mathrm{ACTIVE} \cdot \mathrm{EMPTY}$
		$\cdot \mathrm{ERROR}$
	=	$(\mathrm{OUTPUT\ C} \uparrow \mathrm{OUTPUT\ E}) \uparrow \mathrm{OUTPUT\ G}$
GATEMUXOUT	=	$\overline{\mathrm{OUTPUT}} \cdot \mathrm{ACTIVE} \cdot \mathrm{EMPTY} \cdot (\mathrm{STATUS}$
		$+ \mathrm{READ} \cdot \mathrm{DOUTLOC}) + \mathrm{OUTPUT} \cdot \mathrm{ACTIVE}$
		$\cdot \mathrm{EMPTY} \cdot \overline{\mathrm{ERROR}}$
	=	$(\mathrm{OUTPUT\ B} \uparrow \mathrm{OUTPUT\ H}) \uparrow \mathrm{OUTPUT\ G}$
FULLOUT	=	GATE MUX OUT
KOUTPUT	=	$\mathrm{ACTIVE} \uparrow \overline{\mathrm{EMPTY}}$
MUXOUTLOW	=	$\mathrm{OUTPUT} \cdot \mathrm{ACTIVE} \cdot \mathrm{EMPTY} \cdot \overline{\mathrm{ERROR}}$
	=	$\overline{\mathrm{OUTPUT\ G}}$
DCNOUTA	=	$\overline{\mathrm{ACTIVE} \cdot \mathrm{EMPTY}\ \mathrm{ERROR}\ \mathrm{OUTPUT}}$
		$\mathrm{OUTPUT\ B} \uparrow \mathrm{OUTPUT} \uparrow \mathrm{ERROR}$
SETDCNIN	=	DCNOUT

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: BY: CHECKED: APPROVED: DATE:

TITLE—



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

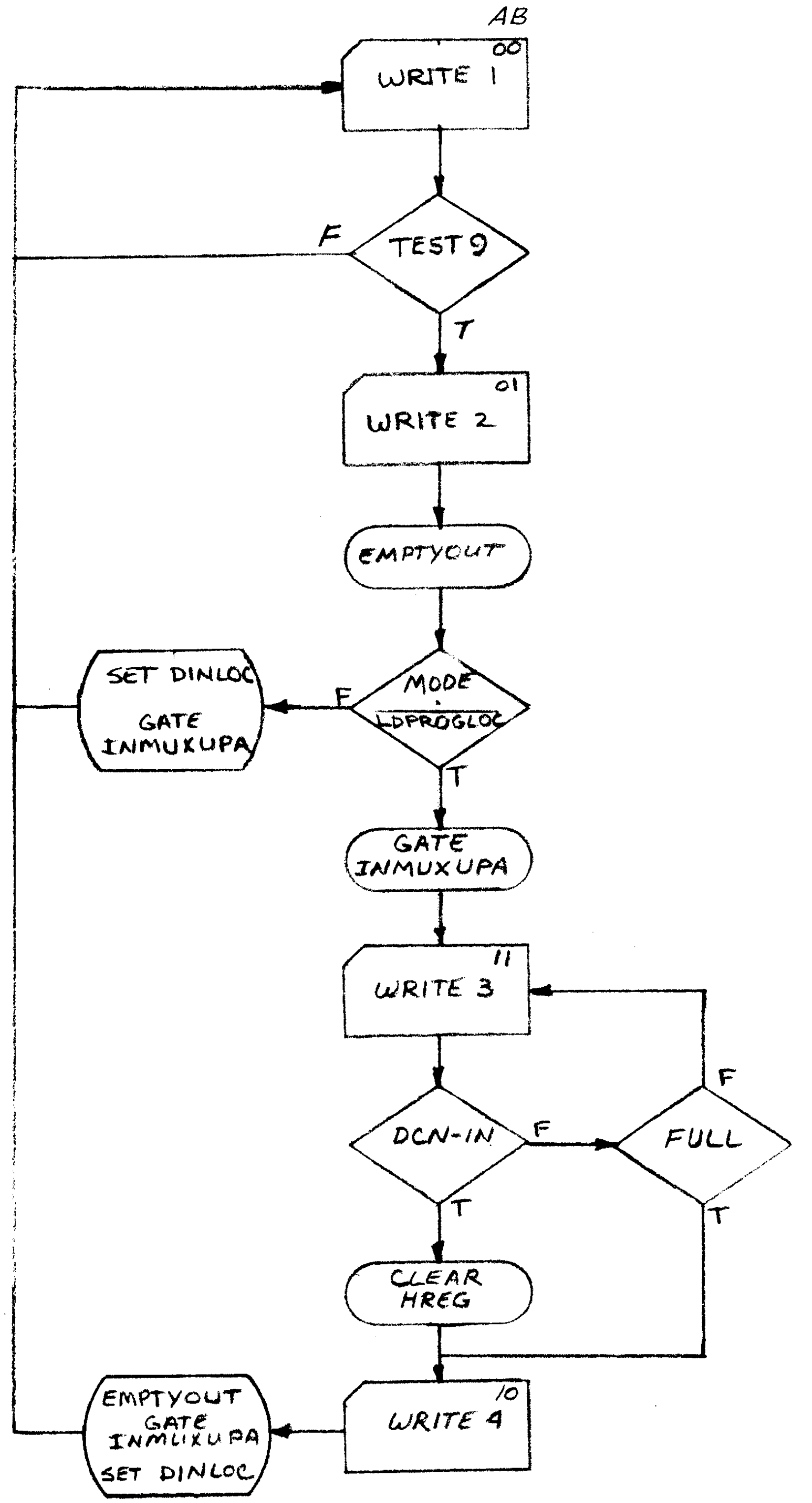
TITLE—

WRITE E	=	$\mathrm{WRITEA} \uparrow \overline{\mathrm{WRITE\ B}}$
WRITE C	=	$\mathrm{WRITEA} \downarrow \overline{\mathrm{WRITE\ B}}$
WRITE D	=	$\overline{\mathrm{LDPROGLOC}} \uparrow \mathrm{MODE}$
JWRITEA	=	$\overline{\mathrm{WRITEA}} \cdot \mathrm{WRITEB} \cdot \overline{\mathrm{LDPROGLOC}} \cdot \mathrm{MODE}$
	=	$\overline{\mathrm{WRITEC}} \uparrow \mathrm{WRITE\ D}$
KWRITEA	=	$\overline{\mathrm{WRITEB}}$
JWRITEB	=	$\overline{\mathrm{WRITEA}} \cdot \mathrm{ACTIVE} \cdot \mathrm{FULL} \cdot \mathrm{DINLOC} \cdot (\overline{\mathrm{WRITELOC}} \downarrow \mathrm{LDPROGLOC})$
	=	$\mathrm{WRITEA} \downarrow \overline{\mathrm{ACTIVE}} \downarrow \overline{\mathrm{FULL}} \downarrow \overline{\mathrm{DINLOC}} \downarrow (\overline{\mathrm{WRITELOC}} \downarrow \overline{\mathrm{LDPROGLOC}})$
GINMUXALL	=	$\overline{\mathrm{WRITEA}} \cdot \mathrm{WRITEB} \cdot (\overline{\mathrm{MODE}} + \mathrm{LDPROGLOC})$
	=	$\overline{\mathrm{WRITE\ C} \uparrow \mathrm{WRITE\ D}}$
KWRITEB	=	$\mathrm{GINMUXALL} + \mathrm{WRITEA} \cdot \mathrm{WRITEB} \cdot (\mathrm{DCNIN} + \mathrm{FULL})$
	=	$\mathrm{GINMUXALL} \uparrow (\mathrm{WRITEA} \uparrow (\overline{\mathrm{DCNIN}} \uparrow \overline{\mathrm{FULL}}))$
EMPTYOUT	=	$\mathrm{WRITEA} \cdot \mathrm{WRITE\ B} + \mathrm{WRITE\ A} \cdot \overline{\mathrm{WRITEB}}$
	=	$\mathrm{WRITEC} \uparrow \mathrm{WRITE\ E}$
JDINLOC	=	$\overline{\mathrm{WRITEA}} \cdot \mathrm{WRITEB} \cdot (\overline{\mathrm{MODE}} + \mathrm{LDPROGLOC}) + \mathrm{WRITE\ A} \cdot \mathrm{WRITE\ B}$
	=	$\mathrm{GINMUXALL} \uparrow \mathrm{WRITEE}$
GINMUXUP	=	$\overline{\mathrm{WRITEA}} \cdot \mathrm{WRITEB} \cdot (\mathrm{MODE} \cdot \overline{\mathrm{LDPROGLOC}})$
	=	$\mathrm{JWRITEA}$
CLHREG	=	$\mathrm{WRITEA} \cdot \mathrm{WRITEB} \cdot \mathrm{DCNIN}$
	=	$\mathrm{WRITEA} \uparrow \mathrm{WRITEB} \uparrow \mathrm{DCNIN}$
GINMUXLW	=	$\mathrm{WRITEA} \cdot \overline{\mathrm{WRITEB}} = \overline{\mathrm{WRITEE}}$

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ____ BY: ____ CHECKED: ____ APPROVED: ____ DATE: ____

TITLE—

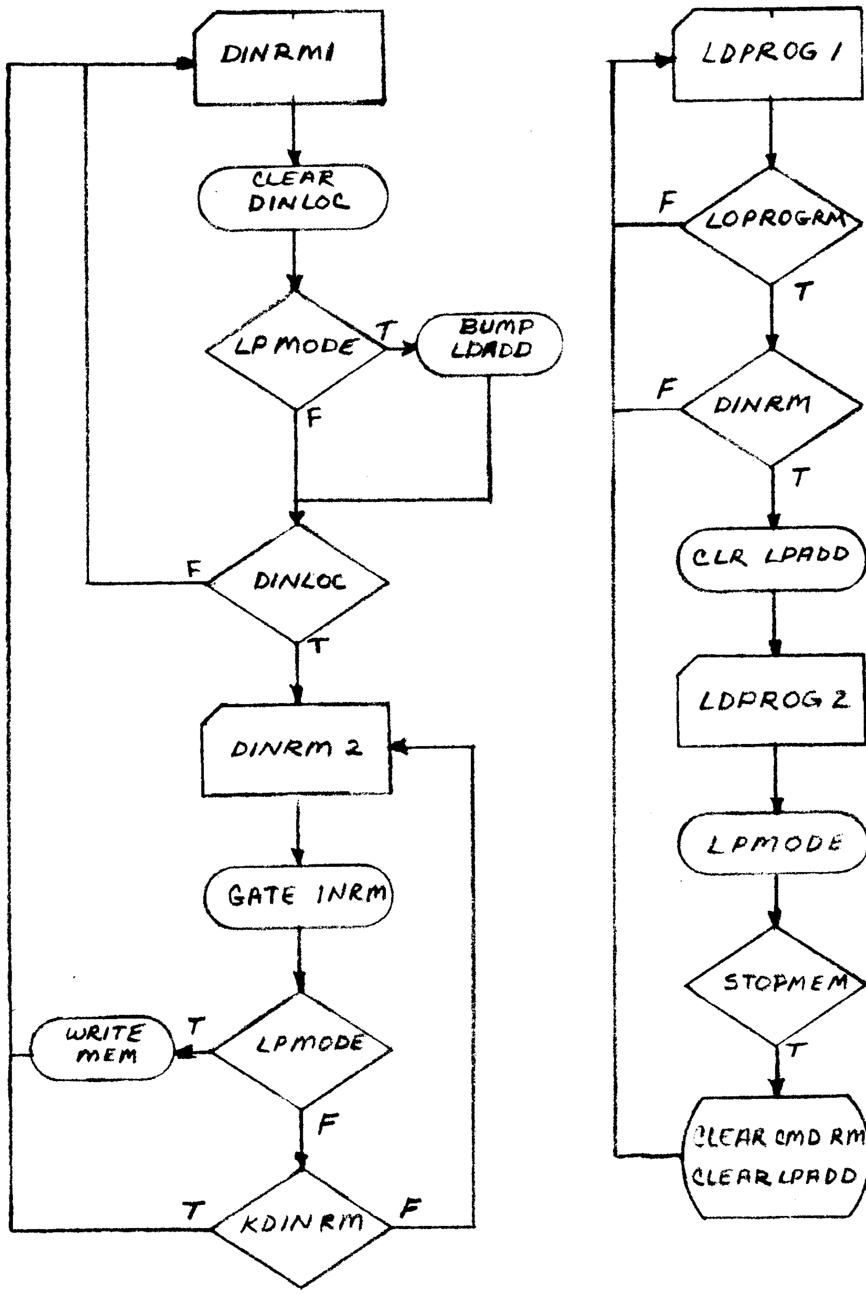


TEST9 = ACTIVE · FULL · $\overline{\text{DINLOC}}$ · (WRITELOC + LDPROGLOC)

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ____ BY: ____ CHECKED: ____ APPROVED: ____ DATE: ____

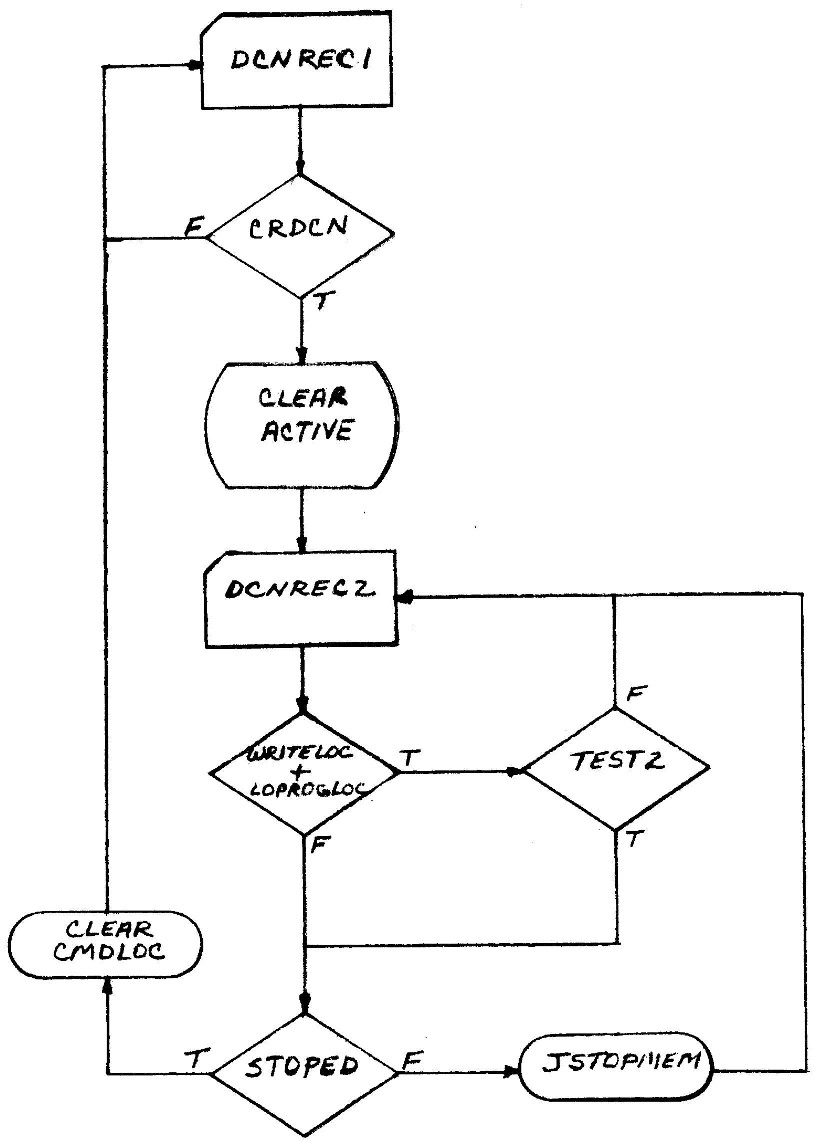
TITLE—



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE—



$$TEST2 = \overline{WRITEA} \cdot \overline{WRITEB} \cdot \overline{DINL\O C} \cdot \overline{DINRM} + WRITERR\O R$$

$$\mathrm{STOPED} = \mathrm{MEMCONT} \downarrow \overline{\mathrm{STOPMEM}}$$

$$\mathrm{RDERROR} = \overline{\mathrm{NONEXISTM}} \uparrow (\mathrm{STOPMEM} \downarrow \mathrm{MEMCONT}) \uparrow (\overline{\mathrm{READRM}} \downarrow \overline{\mathrm{DOUTRM}})$$

$$\mathrm{JMEMCONT} = (\mathrm{NONEXISM} \uparrow (\mathrm{STOPMEM} \downarrow \mathrm{MEMCONT})) \downarrow ((\overline{\mathrm{READRM}} \downarrow \mathrm{DOUTRM}) \downarrow (\overline{\mathrm{WRITERM}} \downarrow \overline{\mathrm{DINRM}}))$$

$$\overline{\mathrm{MEMGO}} = \mathrm{JMEMCONT} \downarrow \mathrm{CKIDONS}$$

$$\mathrm{CLCMDRB} = \mathrm{MEMCONTC} \downarrow \overline{\mathrm{READSET}} \downarrow \overline{(\overline{\mathrm{READRM}} \downarrow \overline{\mathrm{DOUTRM}})}$$

$$\mathrm{MEMCONTC} = \mathrm{MEMCONT} \uparrow \mathrm{MEMDONE}$$

$$\mathrm{MEMDONE} = \mathrm{REQFF} \downarrow \mathrm{SELI}$$

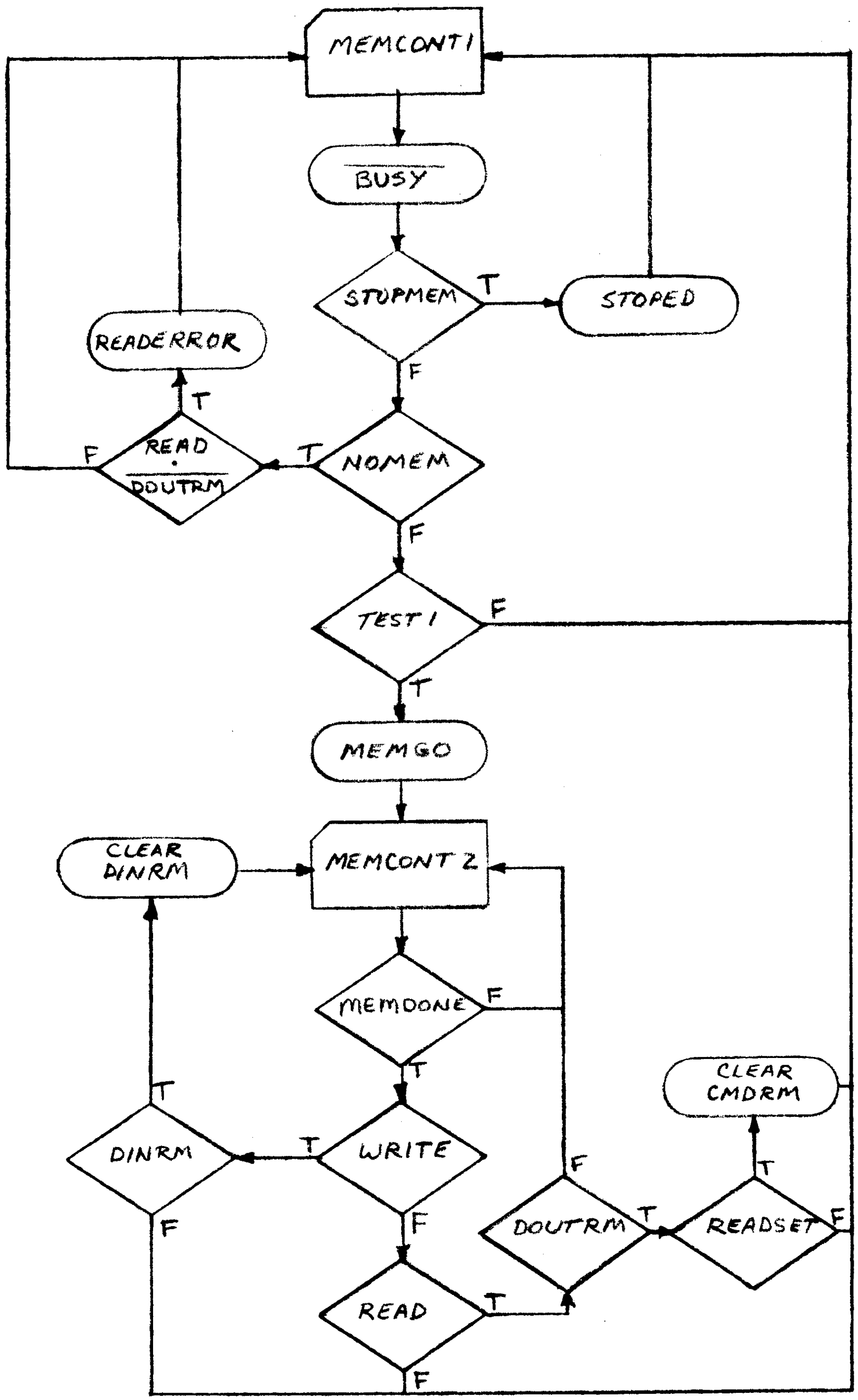
$$\mathrm{KMEMCONT} = \mathrm{MEMCONT} \downarrow ((\overline{\mathrm{READRM}} \downarrow \overline{\mathrm{DOUTRM}}) \downarrow (\overline{\mathrm{WRITERMA}} \downarrow \mathrm{DINRM}) \downarrow (\mathrm{READRM} \downarrow \mathrm{WRITERM}))$$

$$\mathrm{CLCMDRMB} = \overline{(\mathrm{MEMCONTC} \downarrow \overline{\mathrm{WRITERM}} \downarrow \overline{\mathrm{DINRM}})}$$

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: BY: CHECKED: APPROVED: DATE:

TITLE—



$TEST1 = READRM \cdot \overline{DOUTRM} + WRITERM \cdot DINRM$

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FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE—

$$JSELA = \overline{SELB} \uparrow \overline{DESELT}$$

$$DCNOUTD = SELA \uparrow \overline{SELB} \uparrow PAUSE$$

$$KSELA = (SELB \uparrow SELT) \uparrow DCNOUTD$$

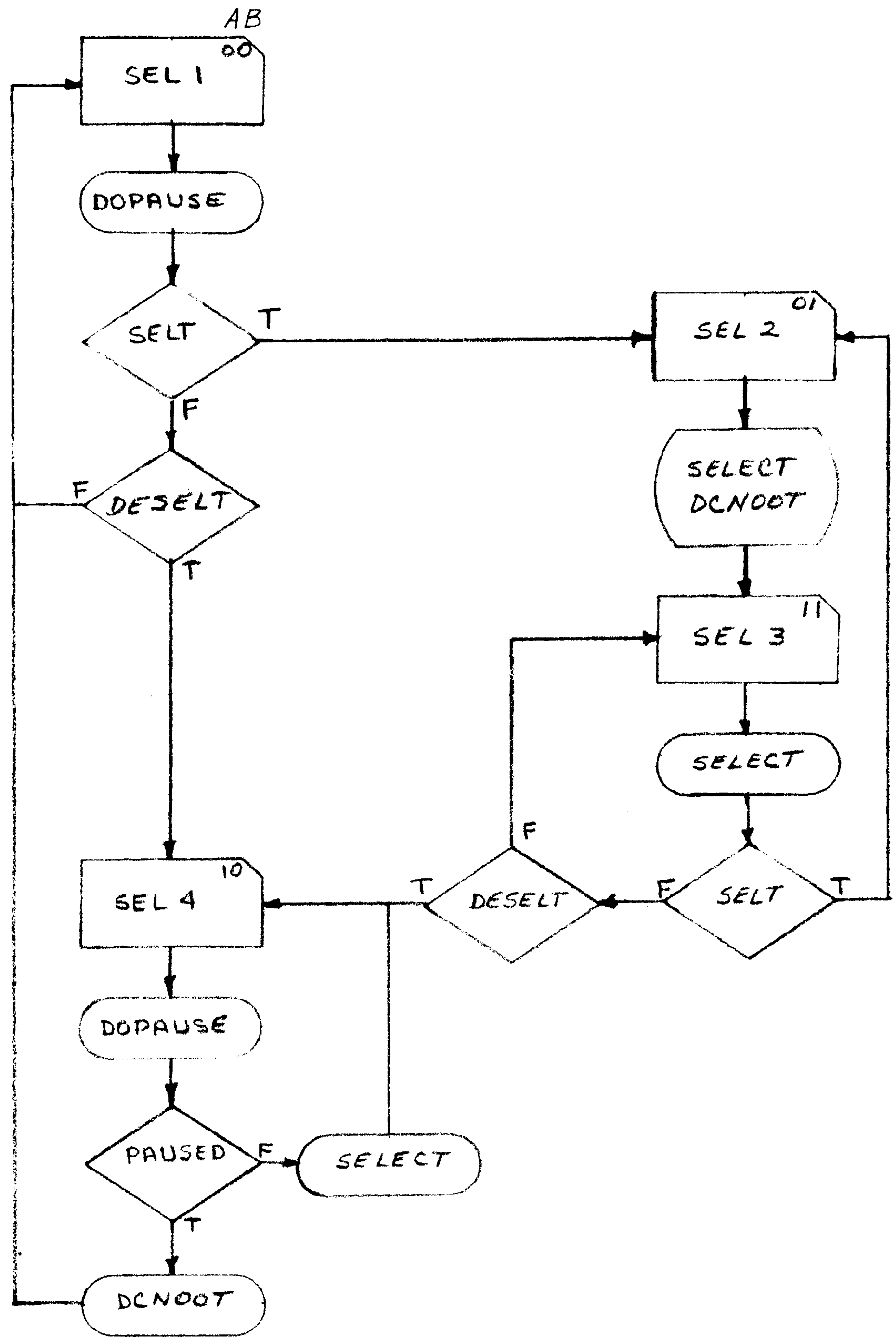
$$JSELB = \overline{SELT} \downarrow SELA$$

$$KSELB = \overline{SELA} \downarrow DESELT$$

$$DCNOUTE = \overline{SELA} \uparrow SELB$$

$$SELECT = (SELA \uparrow PAUSE) \uparrow \overline{SELB}$$

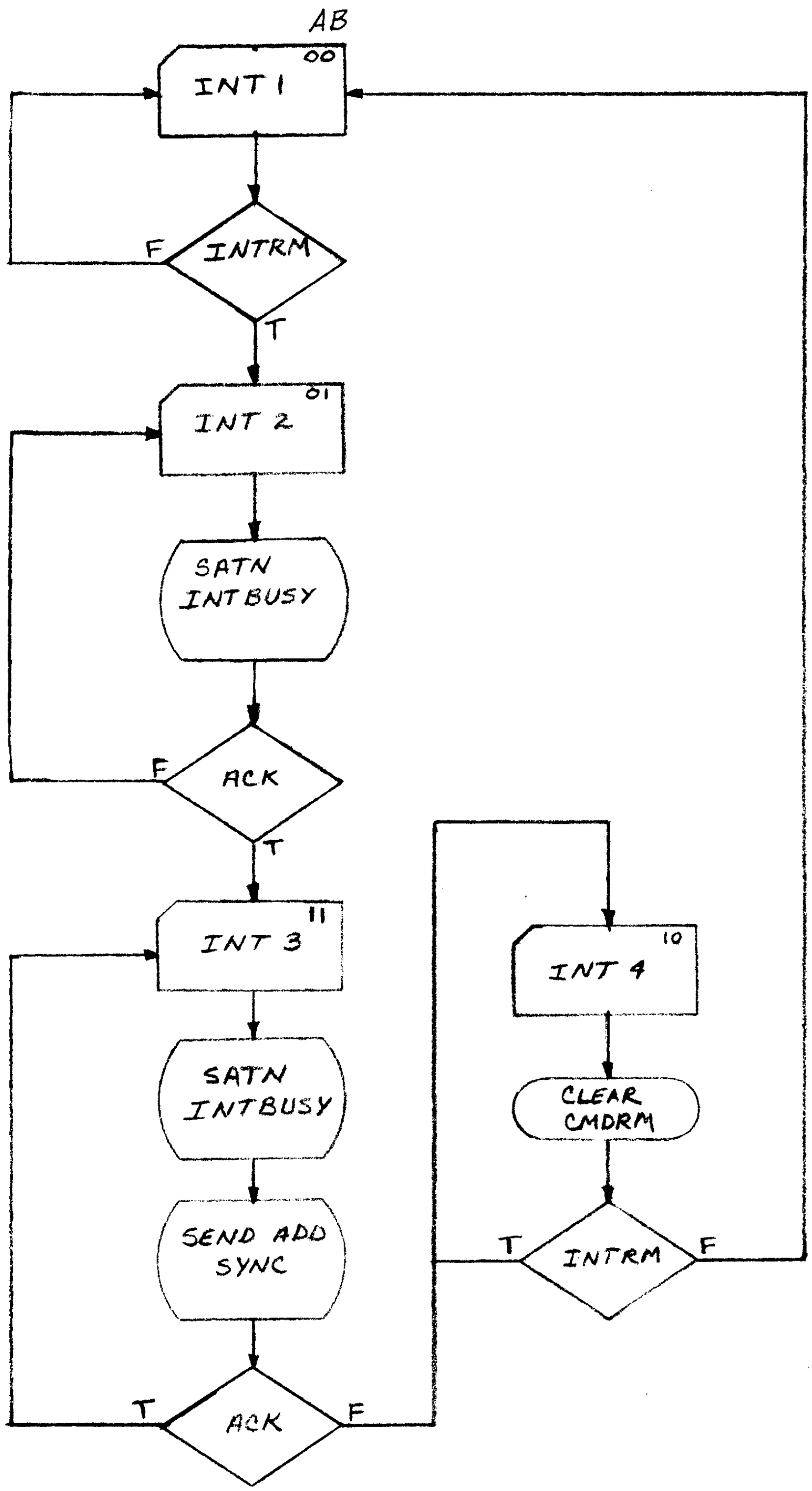
$$DOPAUSE = \overline{SELB}$$



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

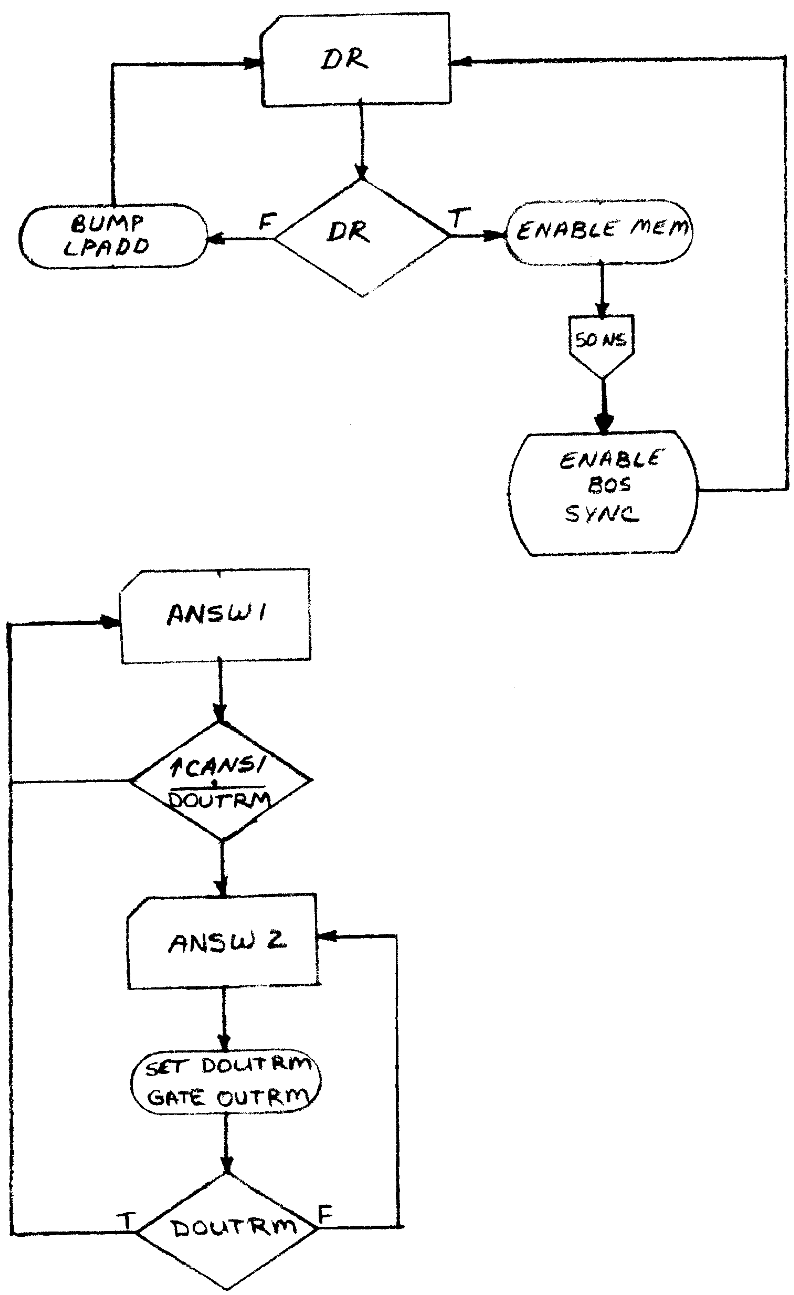
TITLE—



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE—



MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR:____ BY:____ CHECKED:____ APPROVED:____ DATE:____

TITLE—

$FUNCE = CRDCN \uparrow \overline{FUNCA}$

$JFUNCB = CRFUNC \cdot \overline{A}$

$TEST5 = DEC2 + DEC3 = \overline{DEC2} \downarrow \overline{DEC3}$

$FUNCD = TEST5 \downarrow \overline{CRDCN} \downarrow \overline{FUNCA} \downarrow \overline{FUNCB}$

$\overline{CLCONTFF} = \overline{FUNCA} \cdot \overline{FUNCB} = FUNCA \uparrow FUNCB$

$KFUNCB = \overline{FUNCA} \cdot FUNCB \cdot (CRDCN + TEST5)$

$+ FUNCA \cdot FUNCB$

$= FUNCE \uparrow FUNCD \uparrow CLCONTFF$

$TEST6A = (DEC1 + DEC4 + DEC5 + DEC6 +$

$DEC7 + DEC3)$

$= \overline{HREG2} \uparrow \overline{HREG0}$

$FUNCG = TEST6A \uparrow \overline{DCNREC} \uparrow \overline{CRDCN} \uparrow FUNCB$

$JFUNCA = \overline{CRDCN} \cdot TEST6 \cdot STOPED \cdot FUNCB$

$= FUNCG \downarrow STOPED$

$JSTOPMEM = \overline{CROCN} \cdot TEST6 \cdot \overline{STOPED} \cdot \overline{FUNCA}$

$FUNCB$

$= FUNCG \downarrow STOPED \downarrow FUNCA$

$GHREG = FUNCB$

$SINMUXFNC = FUNCB$

$ENBDEC = FUNCA + FUNCB = \overline{FUNCA} \uparrow \overline{FUNCB}$

$GCMDLOC = FUNCA \cdot FUNCB$

$= CLRCONTFF$

$FUNCG = FUNCA \uparrow \overline{FUNCB}$

$DCNOUTB = \overline{\overline{CRDCN} \cdot TESTS \cdot \overline{FUNCA}} \cdot FUNCB$

$= FUNCD$

$DCNOUTC = FUNCA \cdot \overline{FUNCB} = FUNCG$

$LOCMDRM = FUNCA \cdot \overline{FUNCB} = \overline{FUNCA \uparrow \overline{FUNCB}}$

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ____ BY: ____ CHECKED: ____ APPROVED: ____ DATE: ____

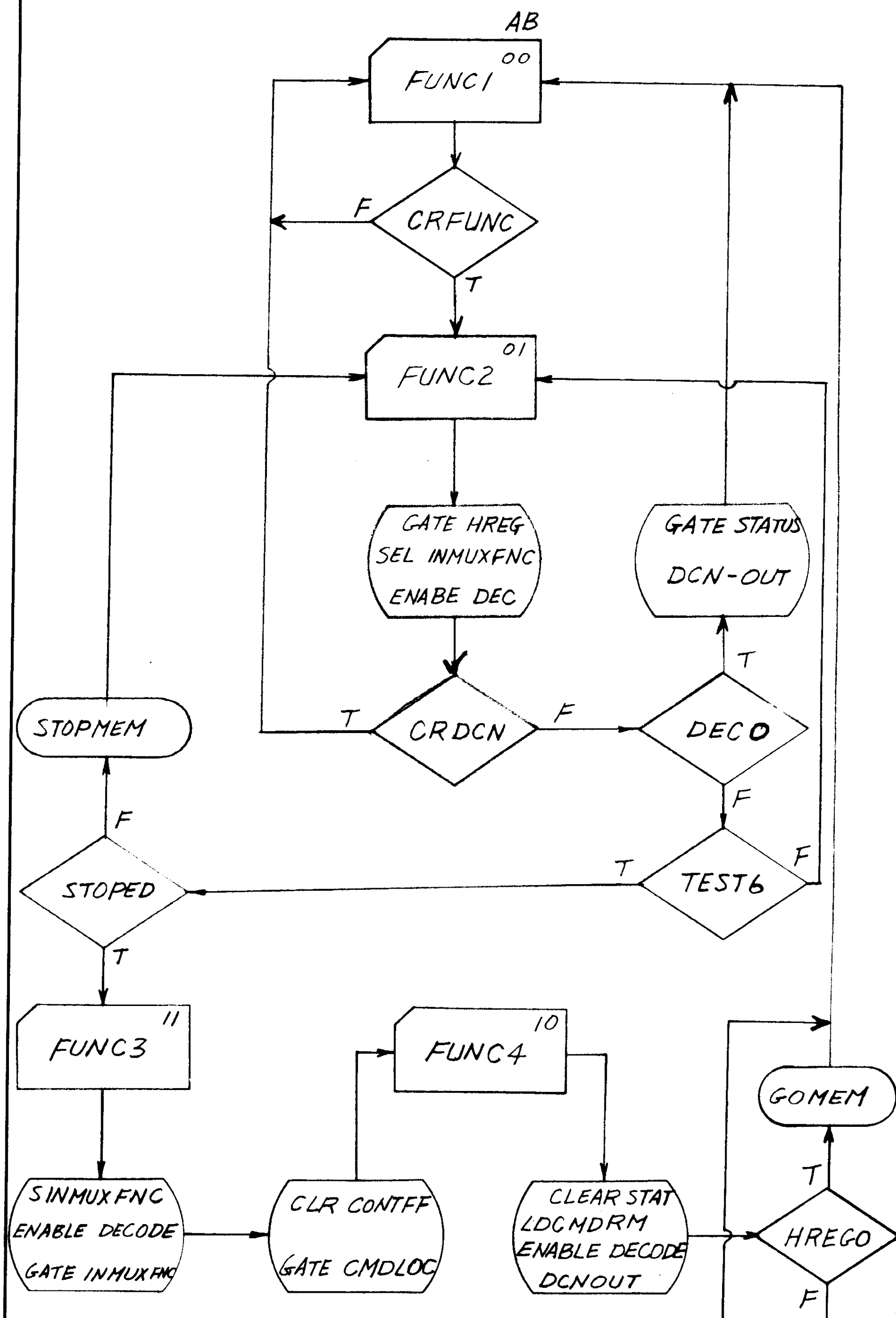
TITLE—

KSTOPMEM = DCNOUTC ↓ $\overline{\text{AREGO}}$

KFUNCA = FUNCB

JSAT = $\overline{\text{FUNCD}}$

KSTAT = LDCMDRM



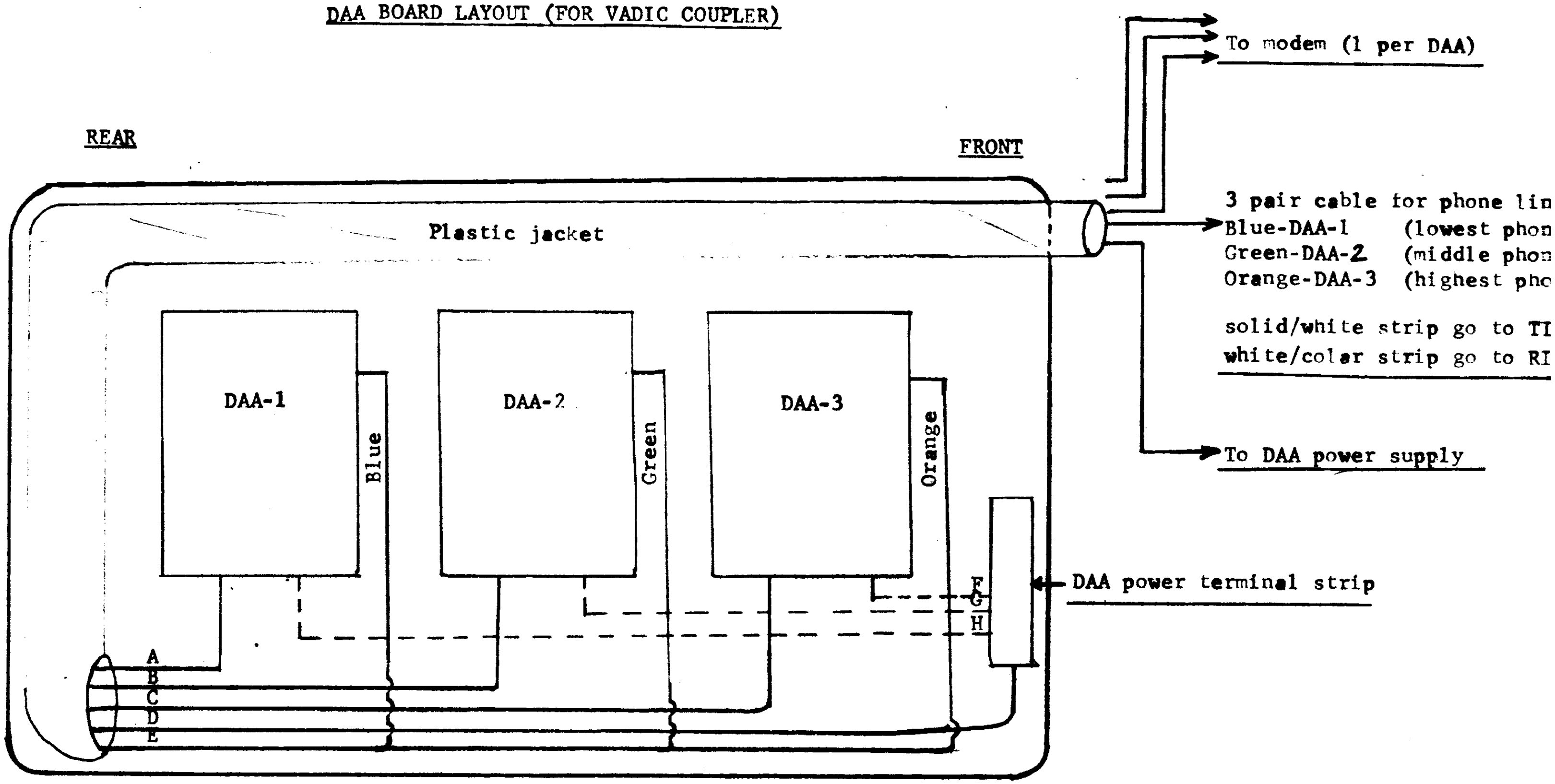
$$TEST6 = (DEC1 + DEC4 + DEC5 + DEC6 + DEC7 + DEC3) \cdot \overline{DCNREC}$$

MICHIGAN STATE UNIVERSITY — COMPUTER LABORATORY

FOR: ______ BY: ______ CHECKED: ______ APPROVED: ______ DATE: ______

TITLE—

DAA BOARD LAYOUT (FOR VADIC COUPLER)



Cable-A,B,C, are modem cable.go to VADIC coupler.
Cable-D is DAA power cable from DAA power supply.
Cable-E is phone line cabel.
Cable-F,G,H, are DAA power cable go to DAA.

11/15/1976 From Peter Chen

B?

7/32 Front-End (B) ?

	1	2	3	4	5	6	7
VADIC-3	VADIC-3A	VADIC-3B		DAA-3A	DAA-3B	EI 200 LINE DRIVER	
	PALS-2		CHASSIS-2A	CHASSIS-2B	CHASSIS-2C		
VADIC-2	VADIC-2A	VADIC-2B	VADIC-2C		DAA-2A		
	PALS-1		CHASSIS-1A	CHASSIS-1B	CHASSIS-1C		
VADIC-1	VADIC-1A	VADIC-1B		DAA-1A	DAA-1B	PUBLIC TERM. LINE DRIVER	
CYBER 750			LMBI CHASSIS-A CHASSIS-B	CPU-B CHASSIS-A CHASSIS-B	CHASSIS-C		
6500		TELERAY	CPU-A CHASSIS-A CHASSIS-B	LMBI CHASSIS-A CHASSIS-B	PALS-0A		

CYBER 750 (CPU)

		1	2	3	4	5	6	7
1	7 CPU-A							
2	6 CPU-B							
3	5 CPU-C							
4	4 MAC							
5	3 MEMORY 1							
6	2 MEMORY 2							
7	1 MEMORY 3							
8	0 MEMORY 4							
9	7							
10	6 CLOCK	TTY						
11	5 BUS SWITCH							
12	4 EDMA							
13	3							
14	2							
15	1							
16	0							
17	7 FRONT-END							
18	6							
19	5							
20	4							
21	3							
22	2							
23	1							
24	0							
25	7							
26	6							
27	5							
28	4 LMBI							
29	3 MEMORY 5							
30	2 MEMORY 6							
31	1 MEMORY 7							
	0 MEMORY 8							

PALS-1 (0XX)

	1	2	3	4	5	6	7	
B SWT (0XX)								
PRINTER (PAF E6)								
PRINTER (PAU E8)			C (BACK CONNECTOR PANNEL)					
COM MUX (A0-AF)	CPS00 (00)	CPS 01 (01)	CPS 02 (02)	CPS 03 (03)	CPS 04 (04)	CPS 05 (05)	CPS 06 (06)	CPS
COM MUX (B0-BF)	CPS08 (08)	CPS09 (09)	CPS 10 (10)	CPS 11 (11)	CPS 12 (12)	CPS 13 (13)	CPS 14 (14)	CPS
ALMC					A (BACK CONNECTOR PANEL			
PALS 1 (30-37)	OPERATOR	00	02	04	00	1A1-01	1A2-02	1A3-
PALS 2 (38-3F)	06	08	10	12	1A4-04	1A5-05	1A6-06	1A7-
PALS 3 (40-47)	14	16	18	20	1A8-08	1A9-09	1A10-10	1A11-
PALS 4 (48-4F)	22	24	26	28	1A12-12	1A13-13	1A14-14	1A15-
PALS 5 (50-57)	30	32	50	52	1A16-16	1B1-17	1B2-18	1B3-
PALS 6 (58-5F)	54	56	58	60	1B4-20	1B5-21	1B6-22	1B7-
PALS 7 (60-67)	62	64	66	68	1B8-24	1B9-25	1B10-26	1B11-
PALS 8 (68-6F)	70	72	74	76	2A1-28	2A5-29	2A9-30	2A13-
PALS 9 (70-77)	78	80	82	84	2B1-00	2B5-01	2B9-02	2B13-
PALS 10 (78-7F)	86	88	3-4850	3-4851	2C1-04	2C5-05	2D1-06	2D3-
PALS 11 (80-87)	3-4852	3-4853	3-4855	~~I/O CRT~~	2D5-08	2D7-09	2D9-10	2D11-
PALS 12 (90-97)	I/O TKR	I/O DGT		I/O CRT ←	12	15	[illegible]	
					B (BACK CONNECTOR PANEL			

PALS-2 (1 X X)

	1	2	3	4	5	6	7	
B SWT (1XX)								
PRINTER (PAF1EG)								
PRINTER (PAU1EB)				F (BACK CONNECTOR PANNEL)				
COMMUX (A0-AF)	SPARE ~~CONSULT.~~	PDP 11/34	SPARE ~~30 TKR~~	SPARE	TELF 1.	TELF2	SPARE	SPARE
ALMC					D (BACK CONNECTOR PANEL)			
PALS 1 (30-37)	SPARE	01	03	05	00	3A1-01	3A2-02	3A3-03
PALS 2 (38-3F)	07	09	11	13	3A4-04	3A5-05	3A6-06	3A7-07
PALS 3 (40-47)	15	17	19	21	3A8-08	3A9-09	3A10-10	3A11-11
PALS 4 (48-4F)	23	25	27	29	3A12-12	3A13-13	3A14-14	3A15-15
PALS 5 (50-57)	31	33	51	53	3A16-16	3B1-17	3B2-18	3B3-19
PALS 6 (58-5F)	55	57	59	61	3B4-20	3B5-21	3B6-22	3B7-23
PALS 7 (60-67)	63	65	67	69	3B8-24	3B9-25	3B10-26	3B11-27
PALS 8 (68-6F)	71	73	75	77	2A3-00	2A7-01	2A11-02	2A15-03
PALS 9 (70-77)	79	81	83	85	2B3-04	2B7-05	2B11-06	2B15-07
PALS 10 (78-7F)	87	89	31779	PT 9	2C3-08	2C7-09	3B16-10	PT9-11
PALS 11 (80-87)	PT 1	PT 2	PT 3	PT 4	PT1-12	PT2-13	PT3-14	PT10-15
PALS 12 (88-8F)	PT 5	PT 6	PT 7	PT 8	PT5-16	PT6-17	PT9-18	PT11-19
PALS 13 (90-97)	ADS 1	ADS 2	ADS 3	CHEM.	ADS1-20	ADS2-21	ADS3-22	CHEM-23
PALS 14 (98-9F)	STATUS	←——	CONSULT ——→	I/O CRT	24	25	26	27
					E (BACK CONNECTOR PANEL)			

AMPAD · EFFICIENCY® LINE No. 4636

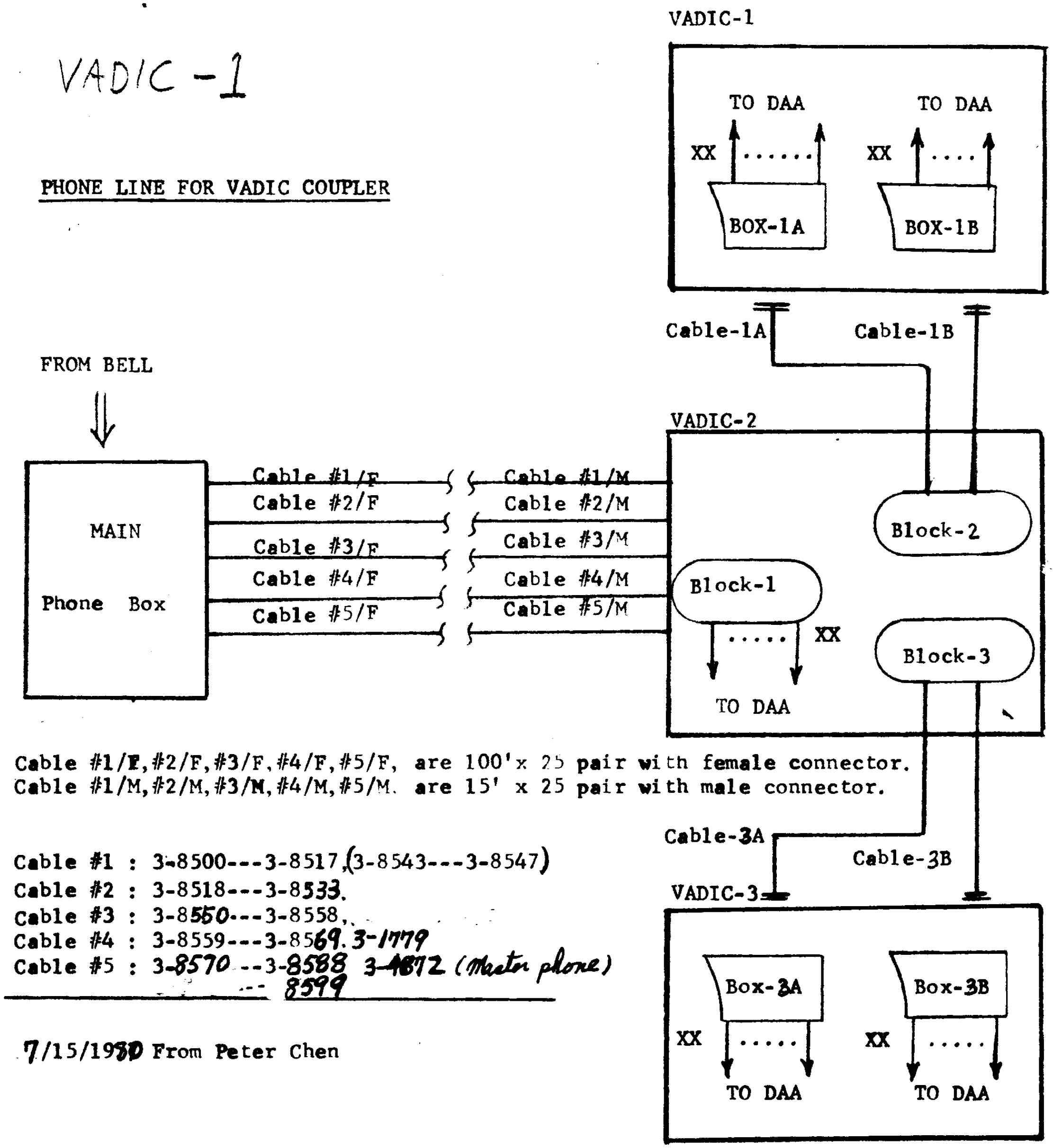
	1	2	3	4	5	6	7
VADIC-1	PALS-1		VADIC-2		PALS-2		VADIC-3
0-300 (EVEN) 38500 - 38530	← 16	4 →	0-1200 38570-38577		← 4	16 →	0-300 (ODD 38501 - 385
0-300 (EVEN) 38532, 38550-38568	← 11	4 →	0-1200 38578-38585		← 4	12 →	0-300 (ODD 38533. 3-17 38551-3856
		2 →	0-1200 38586-38588 38599		← 2		
			35130-35132				
	300 H.W	1200			1200 H.W	300	
	27 23	10			10 25	28	
	60				63		

6500 (PALS-3)

	1	2	3	4	5	6	7	
7 CPU-A								
6 CPU-B								
5 CPU-C								
4 MAC								
3 MEMORY 1								
2 MEMORY 2								
1 MEMORY 3								
0								
7 CLOCK .	TTY							
6 MUX BUS SWITCH								
5 COM MUX (A0-AF)	SYS 1	SYS 2	SYS 3	SYS 4	SYS 5	SYS 6	AP 1	AP 2
4 EDMA								
3								
2 FRONT-END								
1								
0								
7								
6								
5								
4 LMBI								
3 MEMORY 1								
2 MEMORY 2								
1								
7 ALM C								
6 PALS 1 30-37)	UIC 1	UIC. 2	UIC 3	DYK				
5 PALS 2 (38-3F)	35130	35131	35132	OFFICE				
4 PALS 3 (40-47)	ENG 1	ENG 2	ENG 3					
3 PALS 4 (48-4F)	CONF RM ↑	CONF. RM						
2 PALS 5 (50-57)								
1								
0								

VADIC -1

PHONE LINE FOR VADIC COUPLER



Cable #1/F,#2/F,#3/F,#4/F,#5/F, are 100'x 25 pair with female connector.
Cable #1/M,#2/M,#3/M,#4/M,#5/M. are 15' x 25 pair with male connector.

Cable #1 : 3-8500---3-8517,(3-8543---3-8547)
Cable #2 : 3-8518---3-8533.
Cable #3 : 3-8550---3-8558,
Cable #4 : 3-8559---3-8569. 3-1779
Cable #5 : 3-8570 --3-8588 3-4872 (Master phone)
--- 8599

7/15/1980 From Peter Chen

Cable-xx are 3 pair phone c

BOX-1A.1B are 25 pair conne
cting block:
1A:3-8500---3-8546 (EVEN)
1B:3-8550---3-8568 (EVEN)

Cable-1A 1B are 15'x25 pai
with male connector.
1A:3-8500---3-8546 (EVEN)
1B:3-8550---3-8568 (EVEN)

Block-1,2,3. are 50 pair
connecting block.
Block-1:High speed
3-8570---3-8588, 9
Block-2:Low speed
3-8500---3-8568 (EVE
Block-3:Low speed
3-8500---3-8569 (OD

Cable-xx are 3 pair phone c

Cable-3A,3B. are 15'x25 pai
with male connector.
3A:3-8501 ---3-8547 (ODD)
3B:3-8551 ---3-8569, 3-1779(

Cable-xx are 3 pair phone c

Box-3A,3B are 25 pair conne
cting block:
3A:3-8501 --3-8547 (ODD)
3B:3-8551---3-8569, 3-1779(